



# H77H2-M3

Rev : A

ECS  
CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
V A(H61H2-M7)	2011/06/21	Initial version

NOTE:

- 1. Model Code: ED7
- 2. Modified from H61H2-M7 V 1.0

Elitegroup Computer Systems

Title

Cover Page

Size Custom

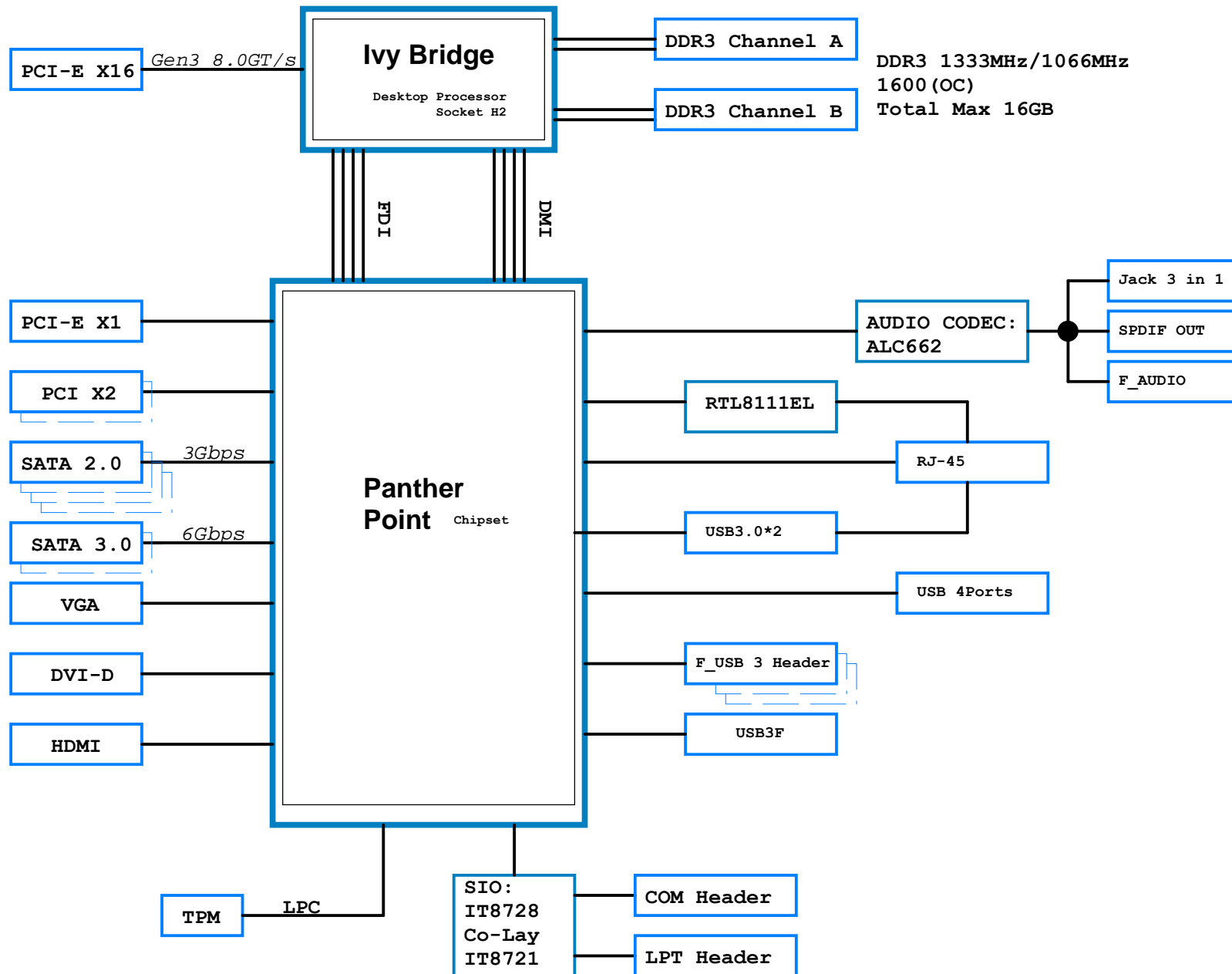
Document Number

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Rev A

Date: Monday, July 18, 2011

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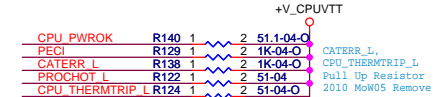
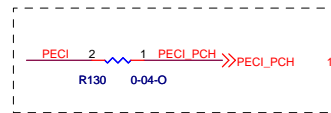
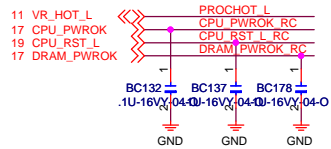
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3	VT1705CD/VT1705CE	GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI

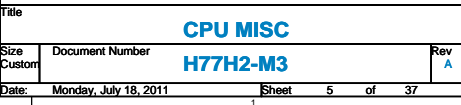
SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16		BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	





CFG[5:6]:  
11=DEFAULT X16,  
01=2X8,  
10=RESERVED,  
00=X8,X4,X4



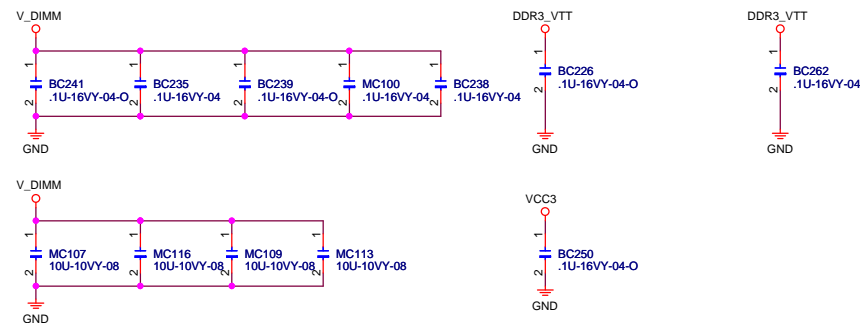
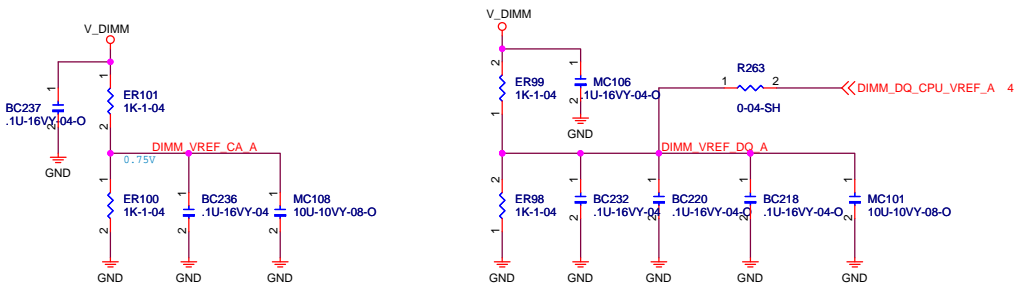
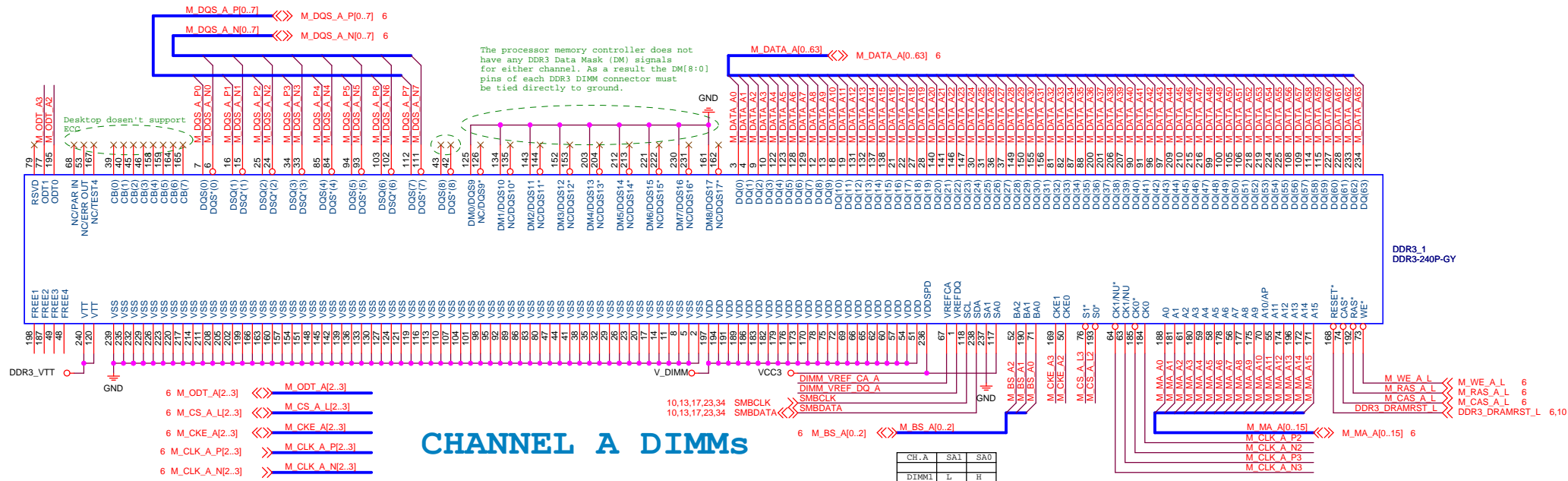


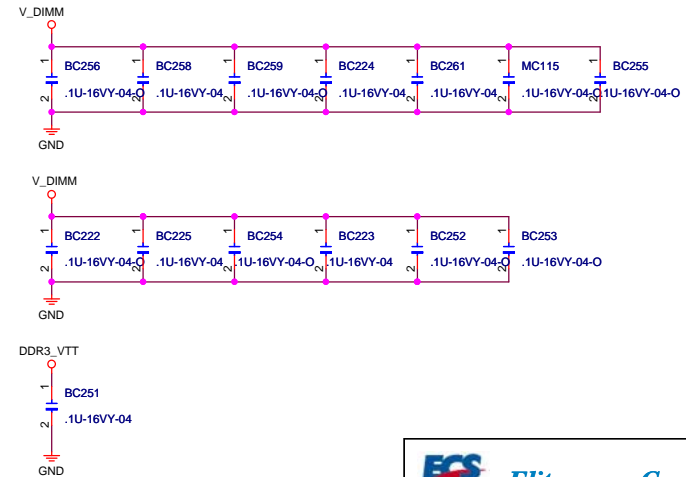
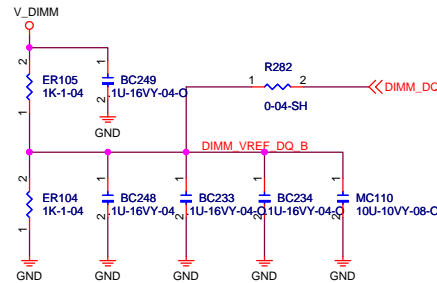
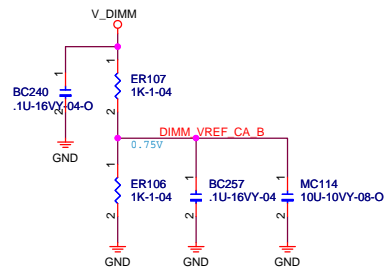
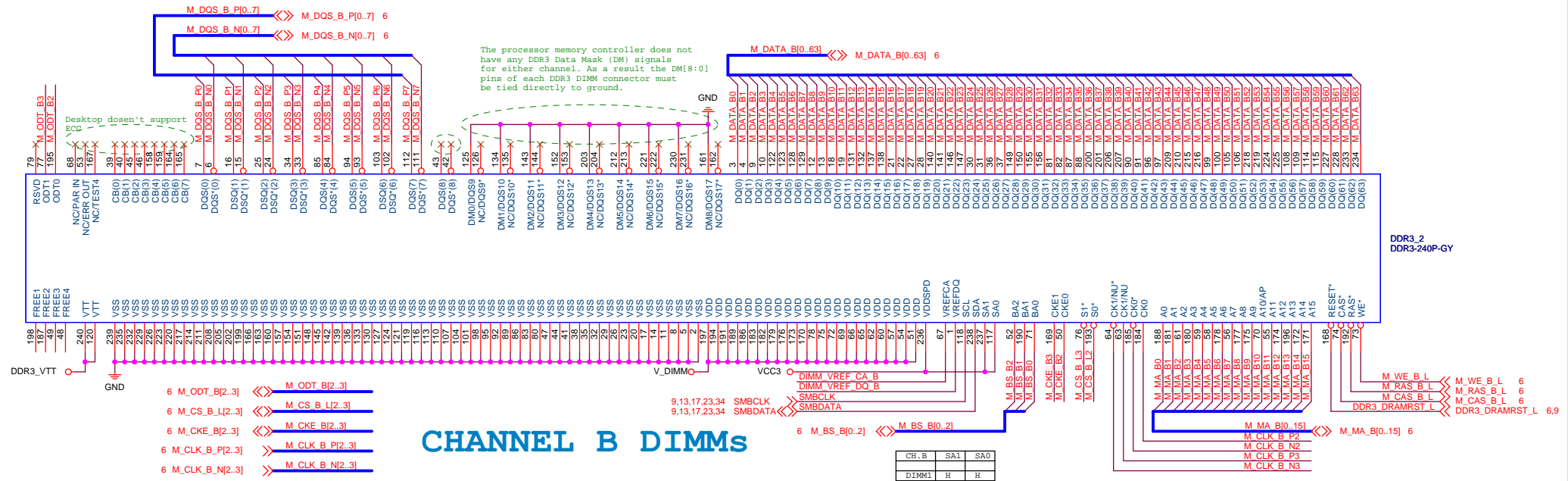


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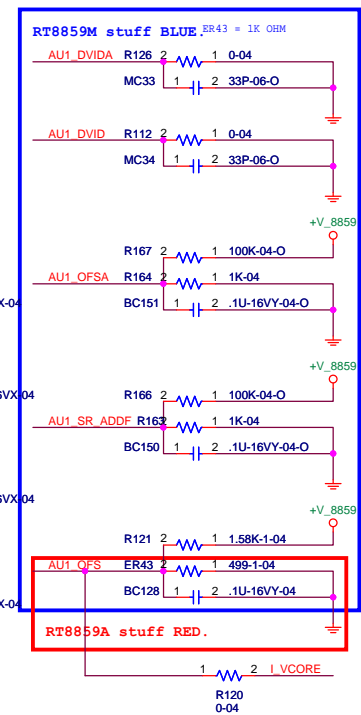
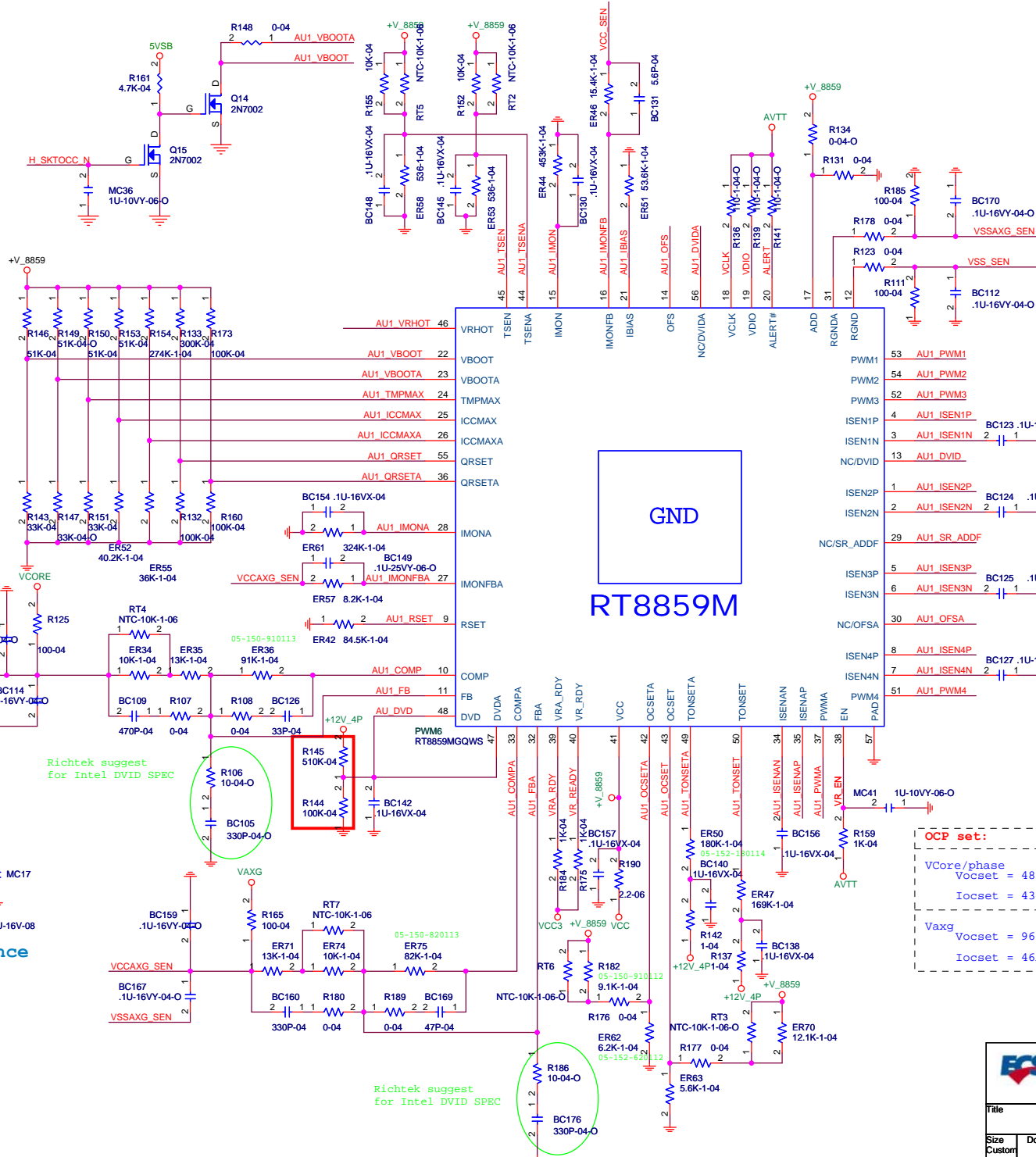
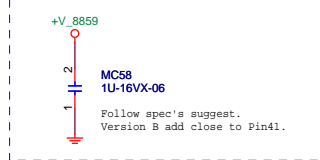
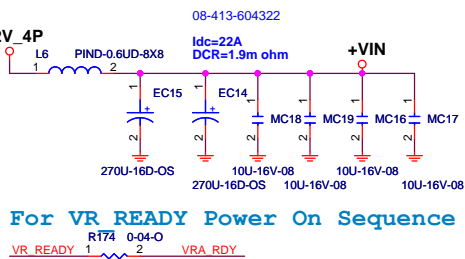
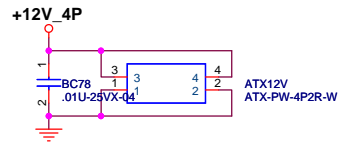
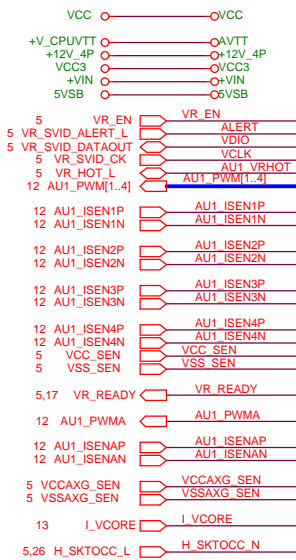








## External Connection



**OCV set:**

$V_{Core}/phase$   
 $V_{ocset} = 48 * I_{ocset} * R_{sense} (DCR)$   
 $I_{ocset} = 43.35A$

$V_{axg}$   
 $V_{ocset} = 96 * I_{ocset} * R_{sense} (DCR)$   
 $I_{ocset} = 46A$

## External Connection



11 AU1\_PWM[1..4] AU1\_PWM[1..4]

11 AU1\_ISEN1P AU1\_ISEN1P

11 AU1\_ISEN1N AU1\_ISEN1N

11 AU1\_ISEN2P AU1\_ISEN2P

11 AU1\_ISEN2N AU1\_ISEN2N

11 AU1\_ISEN3P AU1\_ISEN3P

11 AU1\_ISEN3N AU1\_ISEN3N

11 AU1\_ISEN4P AU1\_ISEN4P

11 AU1\_ISEN4N AU1\_ISEN4N

5,11 VCC\_SEN VCC\_SEN

5,11 VSS\_SEN VSS\_SEN

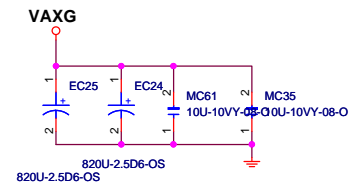
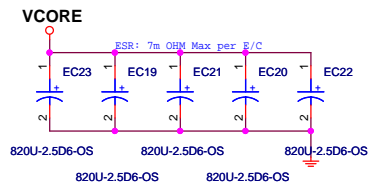
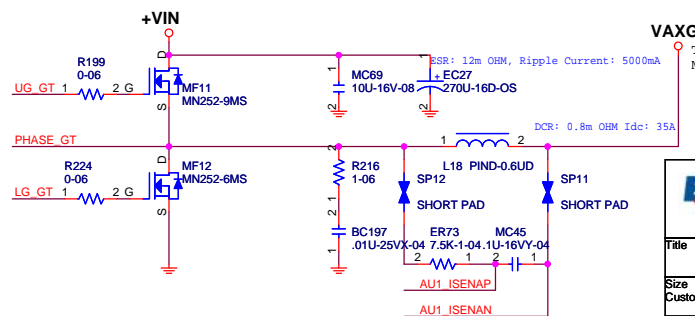
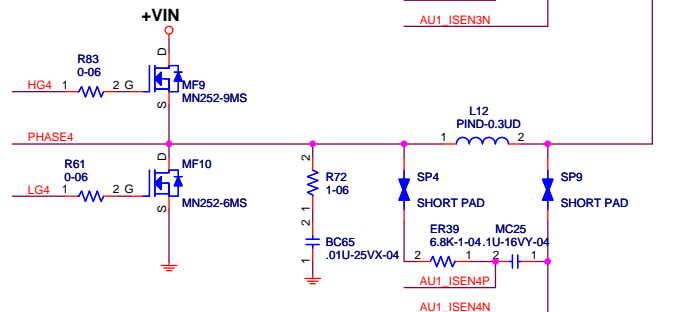
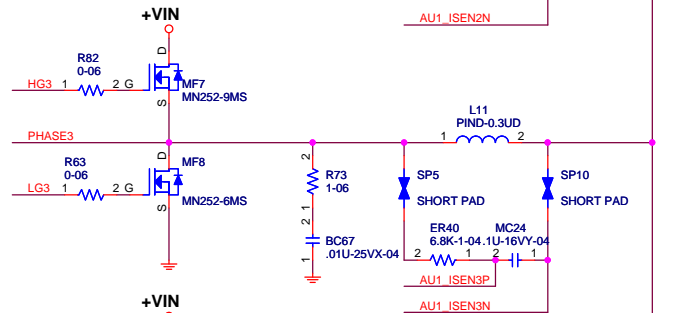
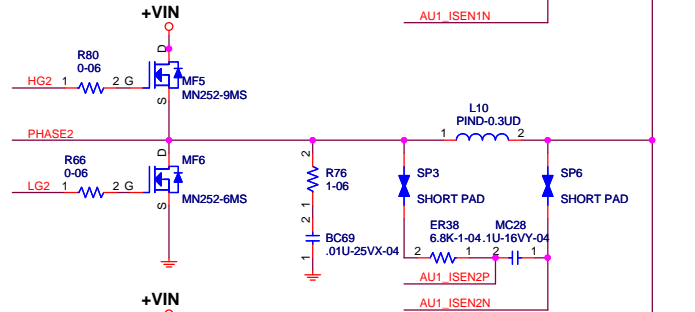
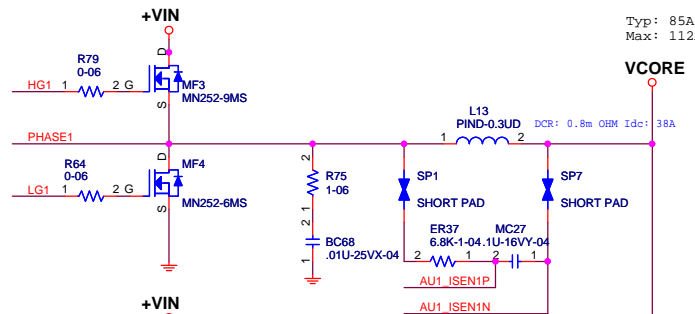
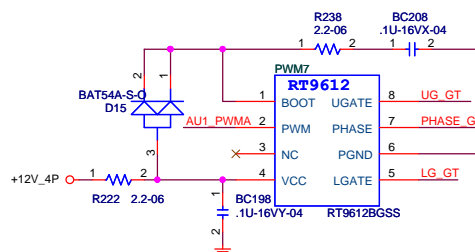
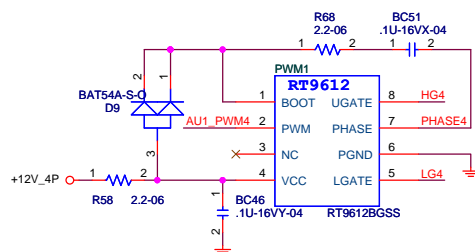
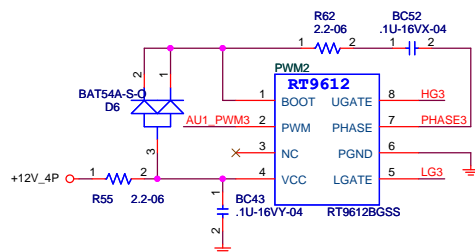
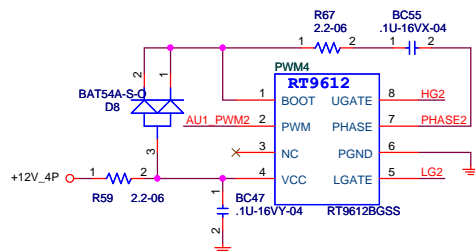
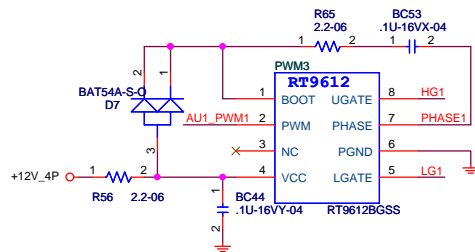
11 AU1\_PWMA AU1\_PWMA

11 AU1\_ISENAP AU1\_ISENAP

11 AU1\_ISENAN AU1\_ISENAN

5,11 VCCAXG\_SEN VCCAXG\_SEN

5,11 VSSAXG\_SEN VSSAXG\_SEN



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Title VCORE & VAXG / RT9612

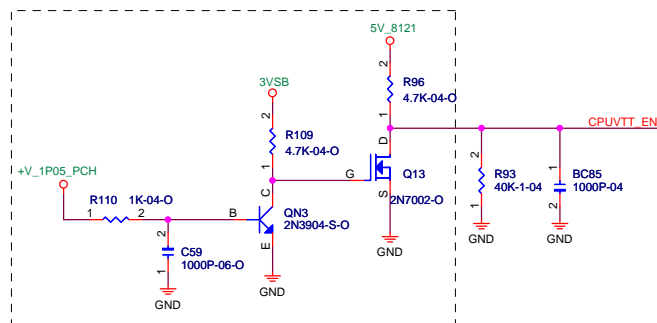
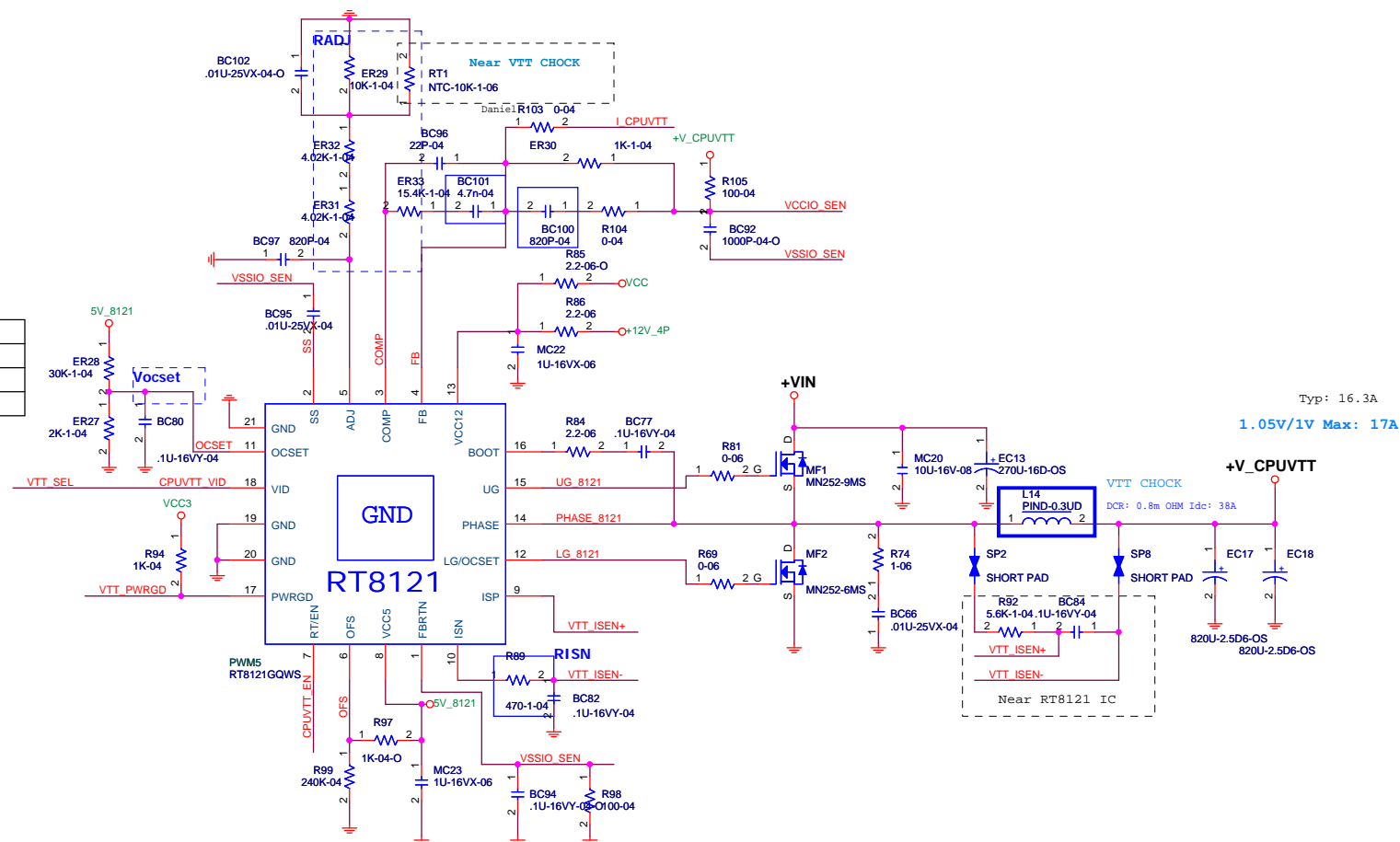
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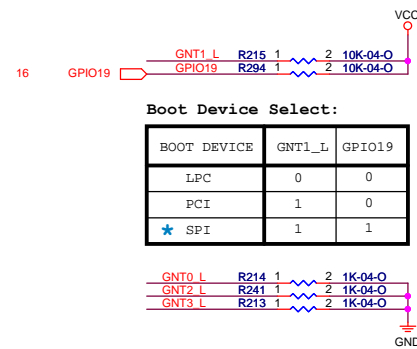
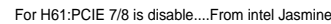
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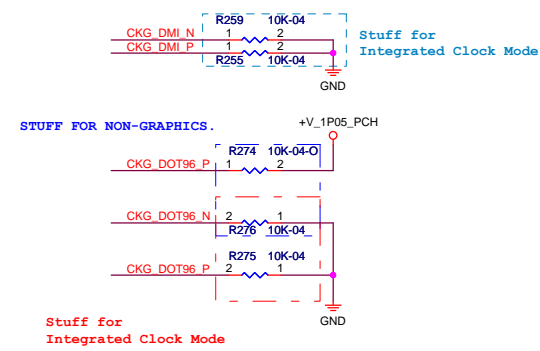
Pin	Function	Pin	Function
1	VCC	1	VCC
2	+12V 4P	2	+12V 4P
3	3VSB	3	3VSB
4	5VSB	4	5VSB
5	+V_1P05_PCH	5	+V_1P05_PCH
6	+V_CPUVTT	6	+V_CPUVTT
7	VTT_SEL	7	VTT_SEL
8	VTT_PWGRD	8	VTT_PWGRD
9	VCCIO_SEN	9	VCCIO_SEN
10	VSSIO_SEN	10	VSSIO_SEN
11	I_CPUVTT	11	I_CPUVTT

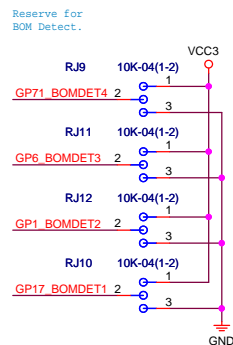
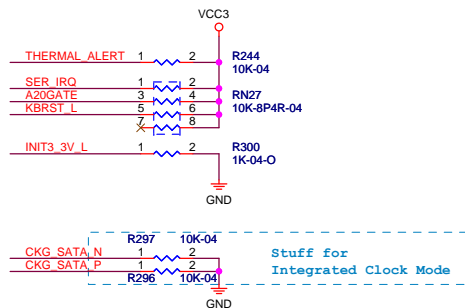
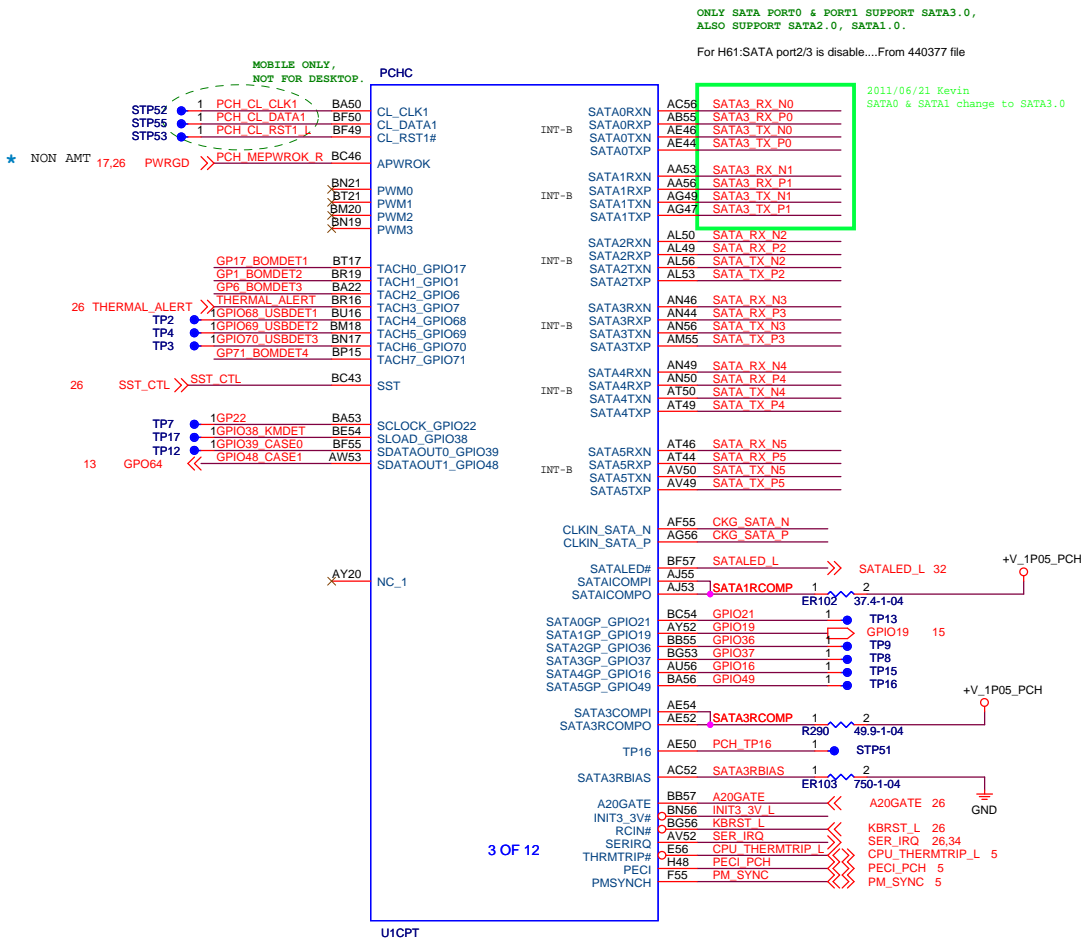
VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V

$$\begin{aligned} \text{Vocset} &= 1/2 * I_x * \text{RADJ} \\ &= 1/2 * (\text{IL} * \text{DCR} / \text{RISN}) * \text{RADJ} \\ \text{Iocset} &= 31.7\text{A} \\ &= 1.82 * \text{Imax} \end{aligned}$$


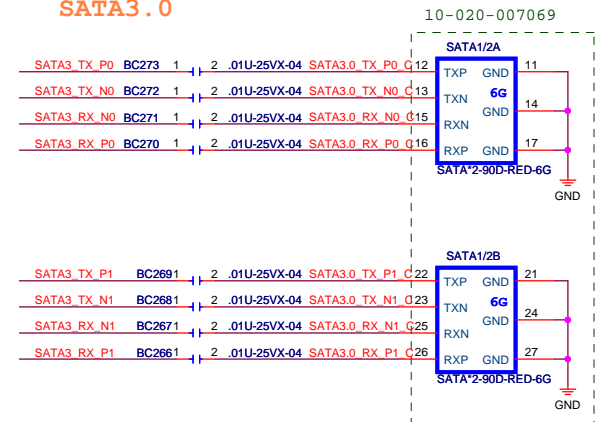


BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
★ SPI	1	1



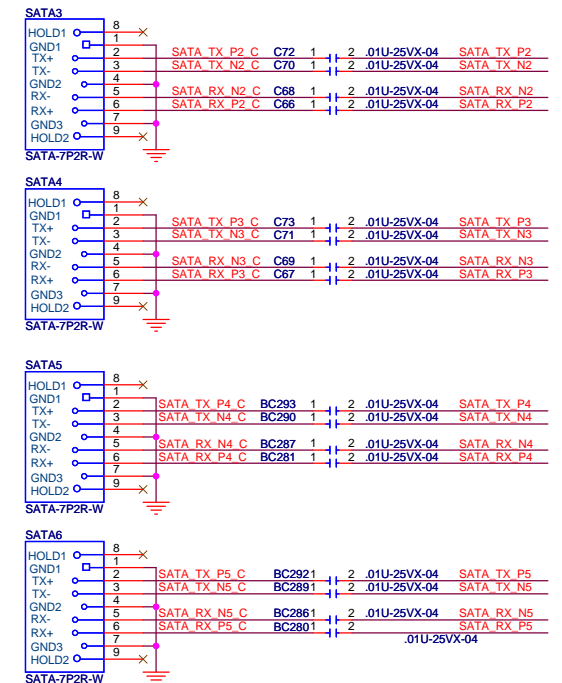


## SATA3.0



Layout Note:  
SATA3.0 4.5/7.5/20 in 85  
Q ±17.5%  
SATA2.0 4.5/7.5/15 in 90  
Q ±17.5%

## SATA2.0



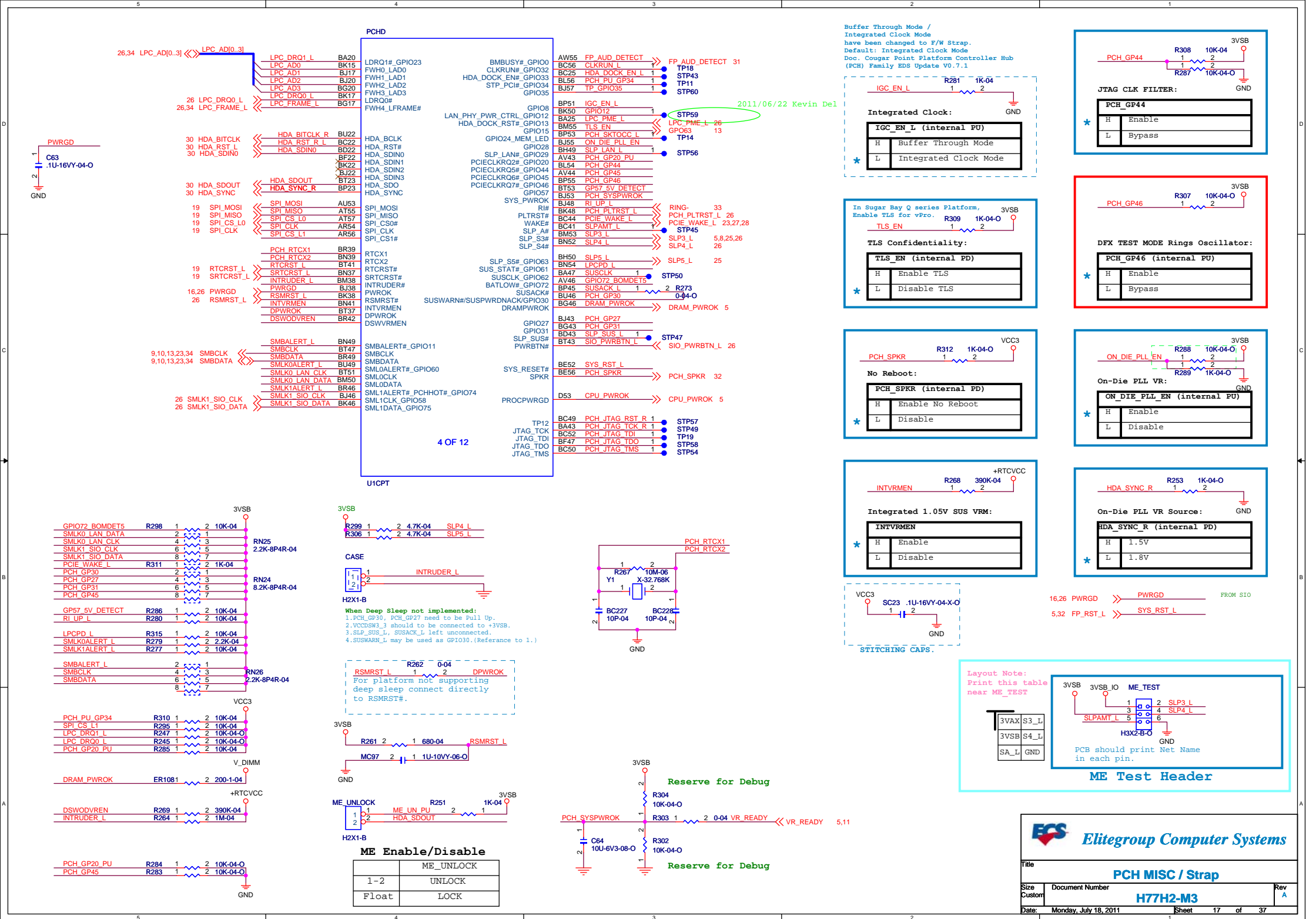
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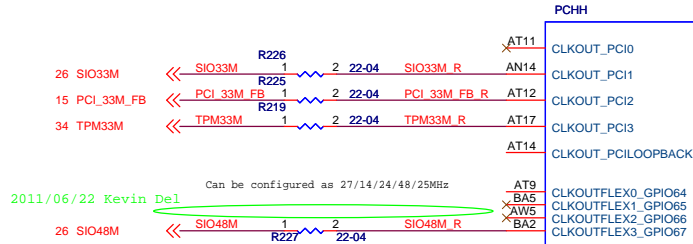
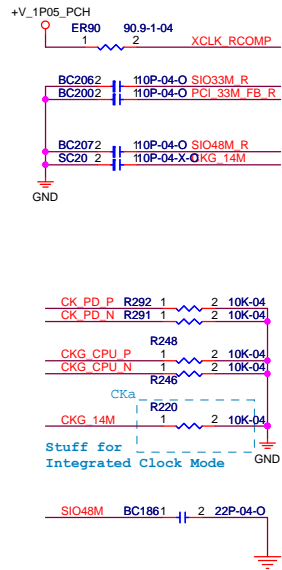
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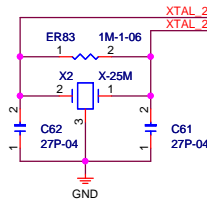
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Layout Note:  
PCI Clock Max 15000MILS



PCHH

CLKOUT\_PCI0  
CLKOUT\_PCI1  
CLKOUT\_PCI2  
CLKOUT\_PCI3  
CLKOUT\_PCILOOPBACK

CLKOUTFLEX0\_GPIO64  
CLKOUTFLEX1\_GPIO65  
CLKOUTFLEX2\_GPIO66  
CLKOUTFLEX3\_GPIO67

XCLK\_RCOMP  
REFCLK14IN

XTAL25\_OUT  
XTAL25\_IN

8 of 12

U1CPT

CLKIN\_GND1\_N R27 CKG\_CPU\_N  
CLKIN\_GND1\_P P27 CKG\_CPU\_P

CLKIN\_GND0\_N W53 CK\_PD\_N  
CLKIN\_GND0\_P V52 CK\_PD\_P

CLKOUT\_ITPXD\_P\_N R52  
CLKOUT\_ITPXD\_P\_P N52

CLKOUT\_PCIE7N AE2  
CLKOUT\_PCIE7P AF1

CLKOUT\_DMI\_N P31 CK\_CPU\_100M\_N  
CLKOUT\_DMI\_P R31 CK\_CPU\_100M\_P

CLKOUT\_DP\_N N56  
CLKOUT\_DP\_P M55

CLKOUT\_PCIE0N AE6 CK\_PE\_100M\_LAN\_L  
CLKOUT\_PCIE0P AC6 CK\_PE\_100M\_LAN\_H

CLKOUT\_PCIE1N AA5 CK\_PE\_100M\_PCI\_L  
CLKOUT\_PCIE1P W5 CK\_PE\_100M\_PCI\_H

CLKOUT\_PCIE2N AB12  
CLKOUT\_PCIE2P AB14

CLKOUT\_PCIE3N AB9  
CLKOUT\_PCIE3P AB8

CLKOUT\_PCIE4N Y9  
CLKOUT\_PCIE4P Y8

CLKOUT\_PCIE5N AF3 PEX1A\_100M\_N  
CLKOUT\_PCIE5P AG2 PEX1A\_100M\_P

CLKOUT\_PCIE6N AB3  
CLKOUT\_PCIE6P AA2

CLKOUT\_PEG\_A\_N AG8 PEX16\_100M\_N  
CLKOUT\_PEG\_A\_P AG9 PEX16\_100M\_P

CLKOUT\_PEG\_B\_N AE12  
CLKOUT\_PEG\_B\_P AE11

to CPU

to LAN

to PCI

2011/06/22 Kevin Del

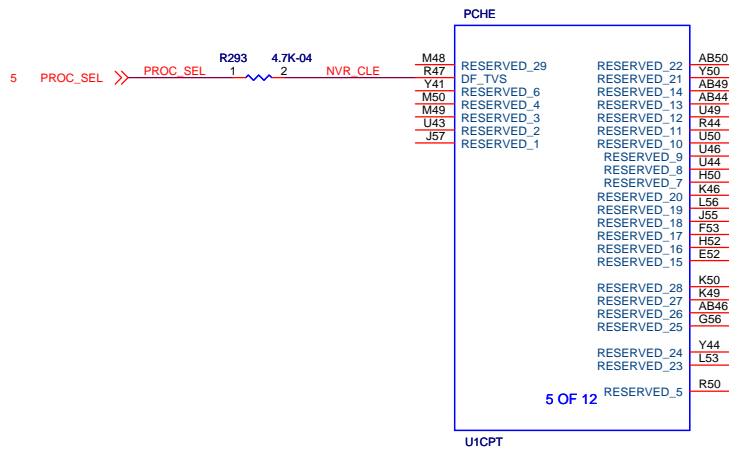
to SLOT

to X16 SLOT



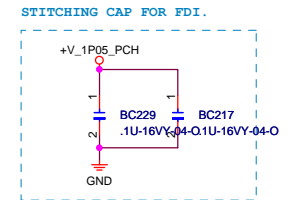
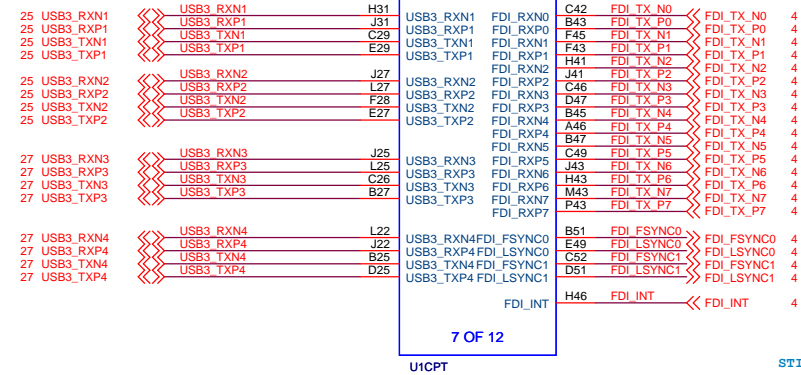
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Rev	A		

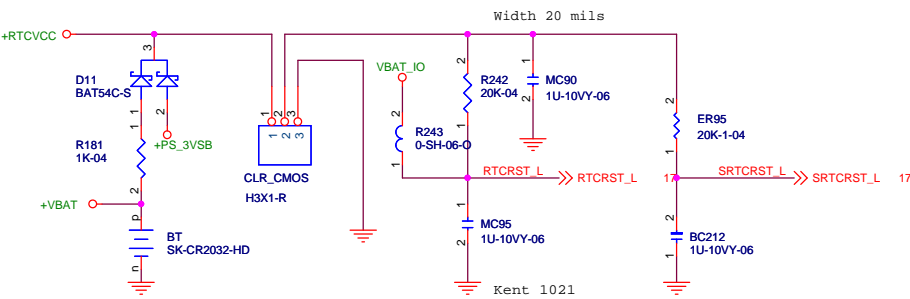


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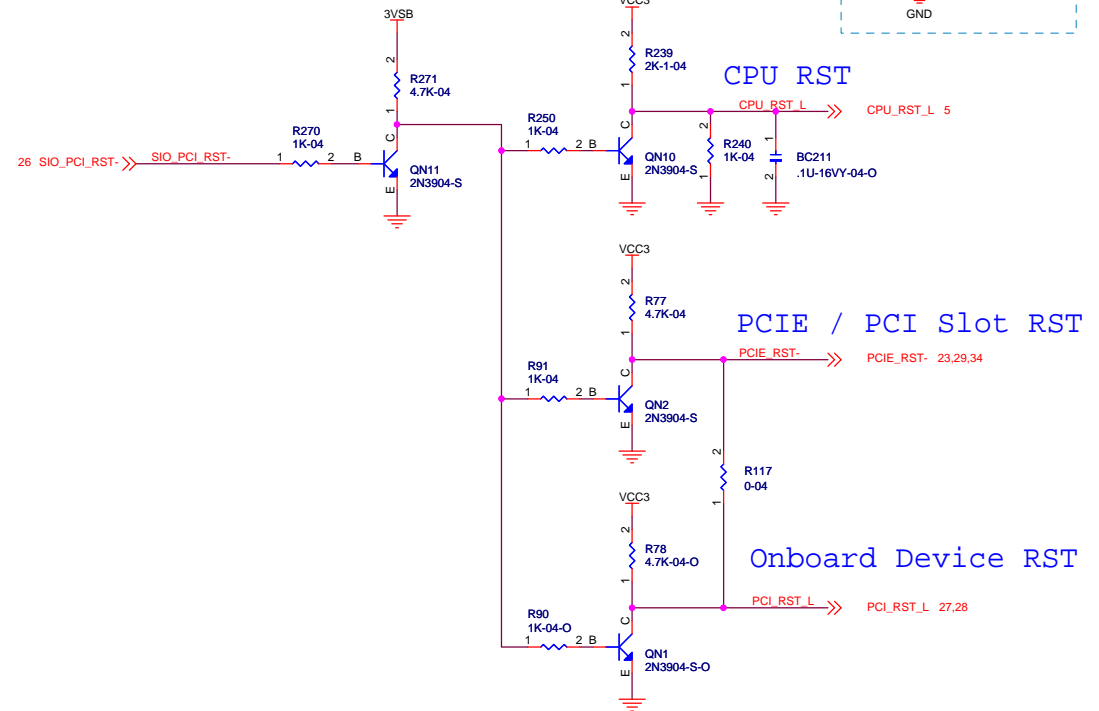
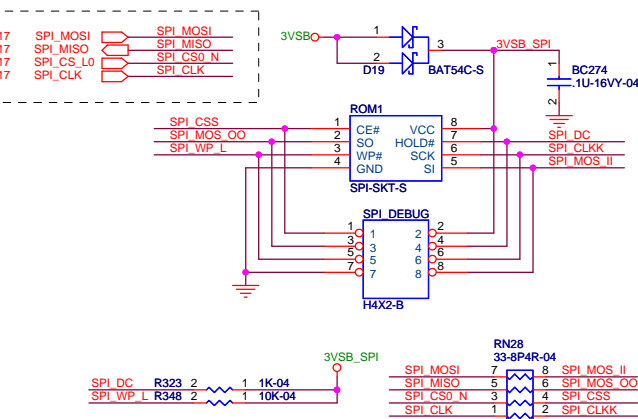
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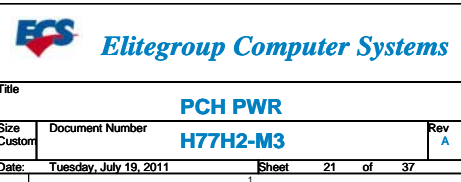
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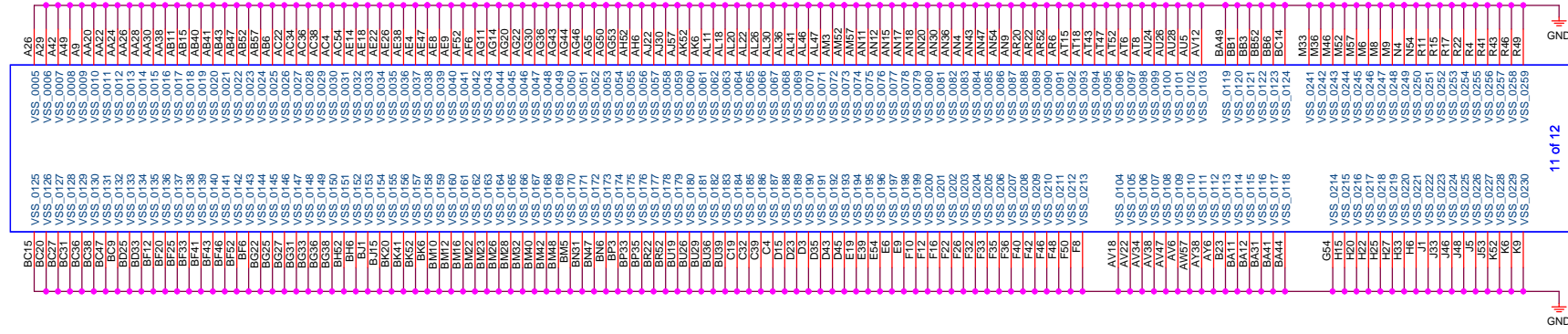
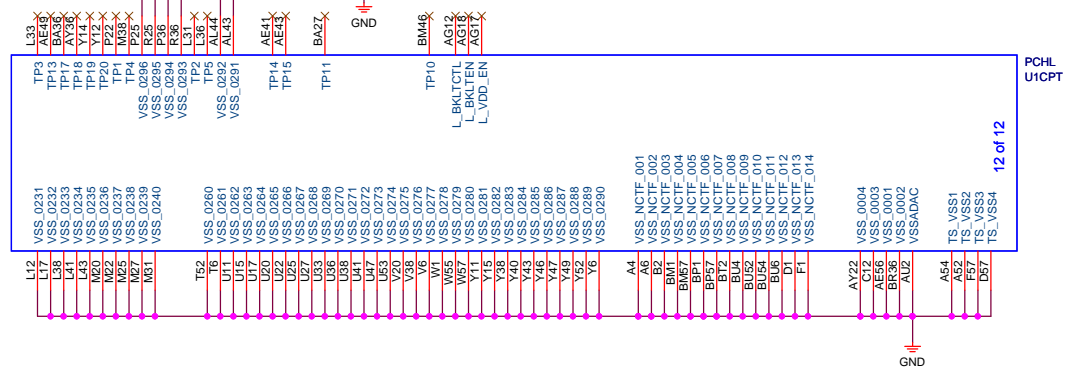


## SPI



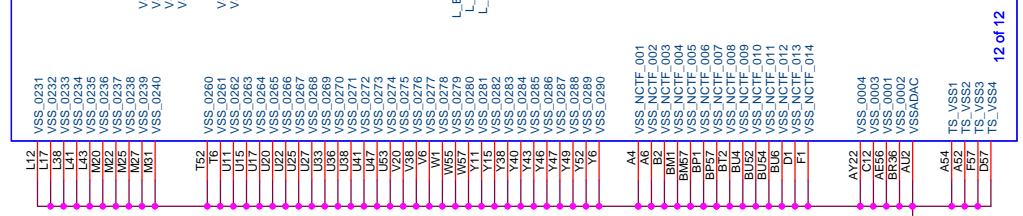






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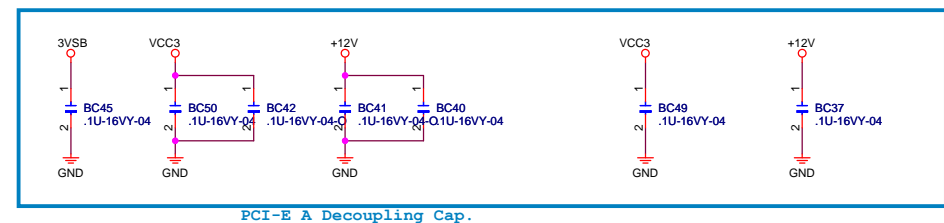
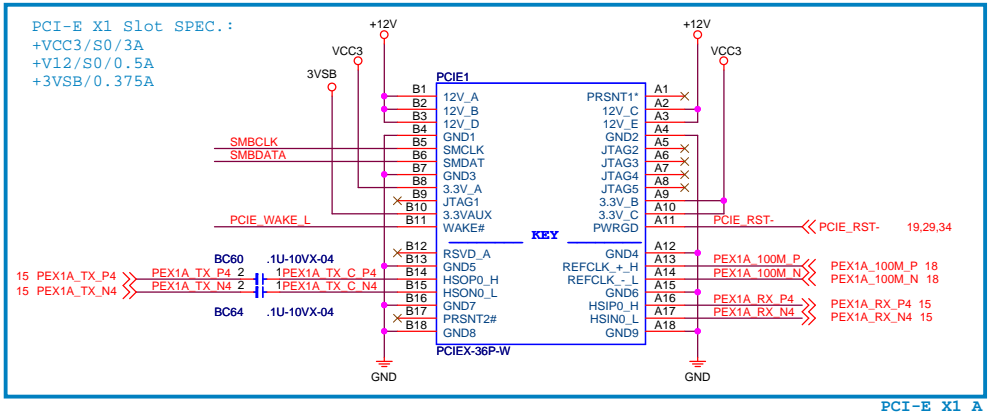
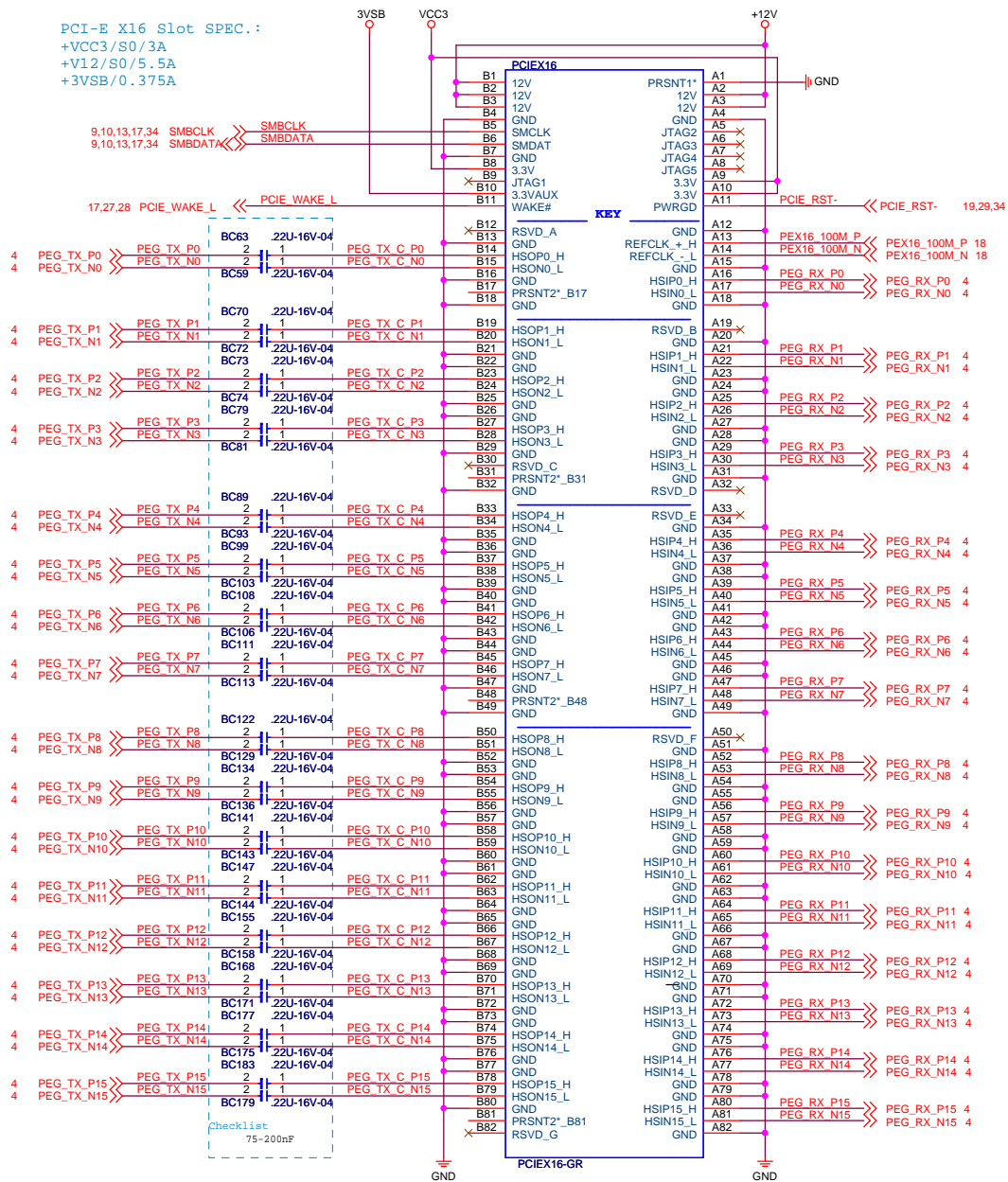
PCHK  
U1CPT



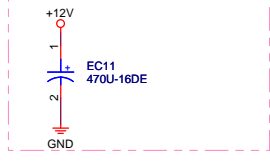
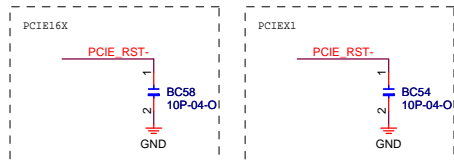
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PCHL  
U1CPT

PCI-E X16 Slot SPEC.:  
+VCC3/S0/3A  
+V12/S0/5.5A  
+3VSB/0.375A



Between PEX16 & PEX1

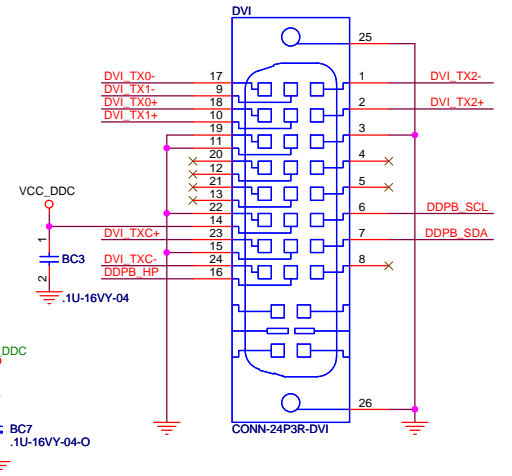
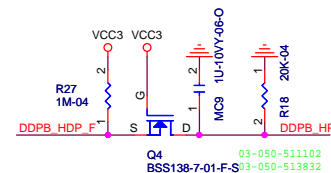
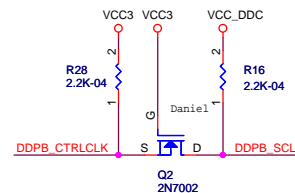
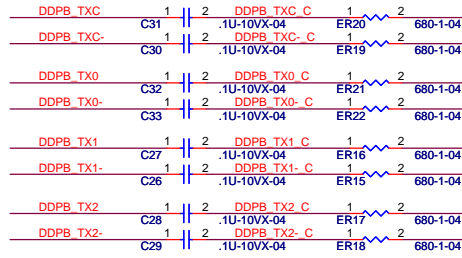




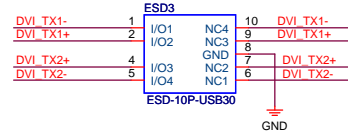
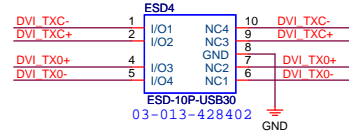
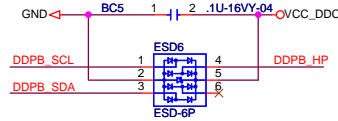
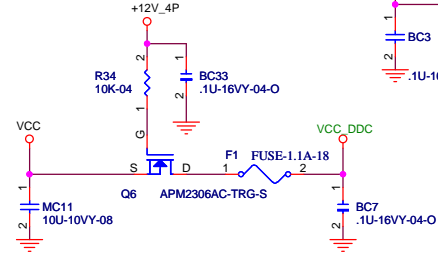
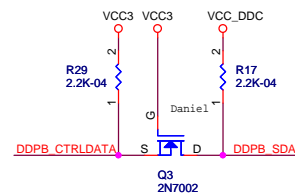
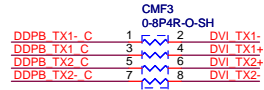
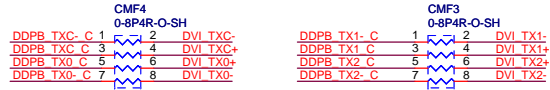
## External Connection

20 DDPD\_HDP\_F << DDPB\_HDP\_F  
20 DDPD\_CTRLCLK << DDPB\_CTRLCLK  
20 DDPD\_CTRLDATA << DDPB\_CTRLDATA

20 DDPD\_TX0 << DDPB\_TX0  
20 DDPD\_TX0- << DDPB\_TX0-  
20 DDPD\_TX1 << DDPB\_TX1  
20 DDPD\_TX1- << DDPB\_TX1-  
20 DDPD\_TX2 << DDPB\_TX2  
20 DDPD\_TX2- << DDPB\_TX2-  
20 DDPD\_TXC << DDPB\_TXC  
20 DDPD\_TXC- << DDPB\_TXC-



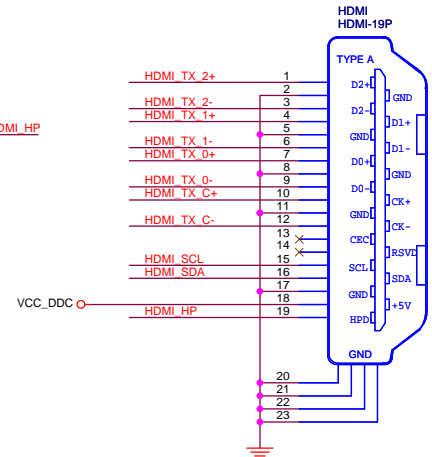
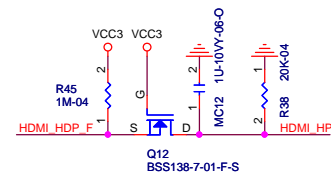
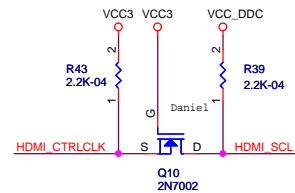
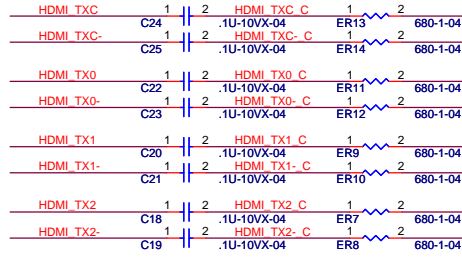
## DVI



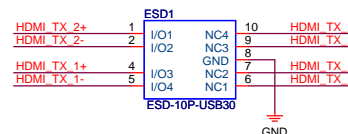
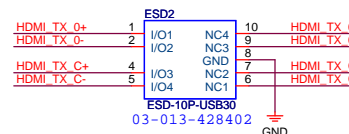
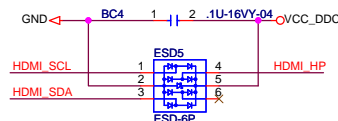
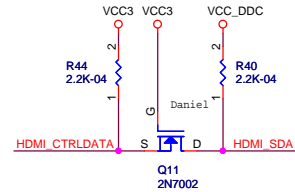
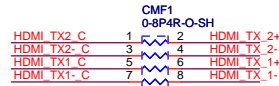
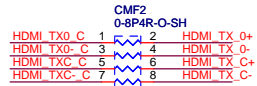
## External Connection

20 HDMI\_HDP\_F << HDMI\_HDP\_F  
20 HDMI\_CTRLCLK << HDMI\_CTRLCLK  
20 HDMI\_CTRLDATA << HDMI\_CTRLDATA

20 HDMI\_TX0 << HDMI\_TX0  
20 HDMI\_TX0- << HDMI\_TX0-  
20 HDMI\_TX1 << HDMI\_TX1  
20 HDMI\_TX1- << HDMI\_TX1-  
20 HDMI\_TX2 << HDMI\_TX2  
20 HDMI\_TX2- << HDMI\_TX2-  
20 HDMI\_TXC << HDMI\_TXC  
20 HDMI\_TXC- << HDMI\_TXC-

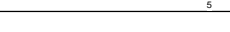
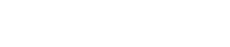
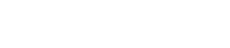
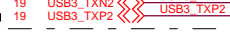
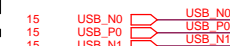
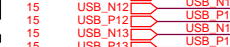
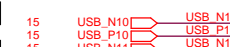
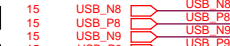
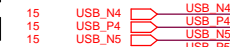


## HDMI



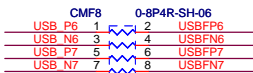


## External Connection

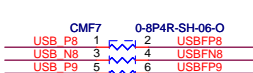


2011/07/11 Kevin Del

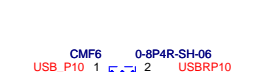
## FRONT\_SIDE



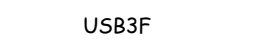
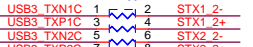
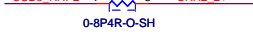
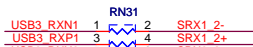
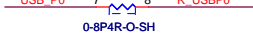
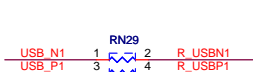
## FRONT\_SIDE



## FRONT\_SIDE

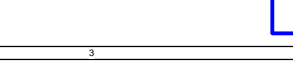
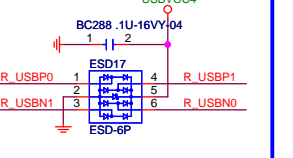
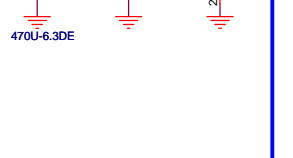
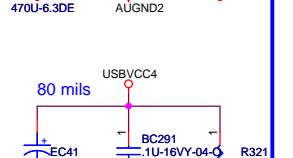
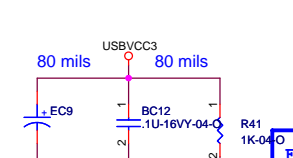
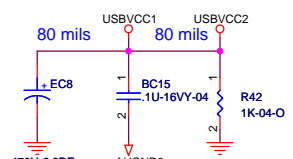
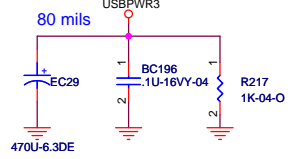
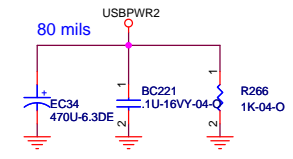
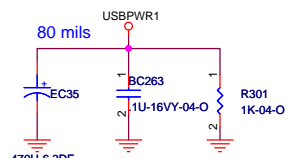
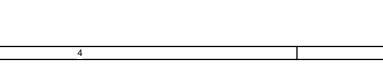
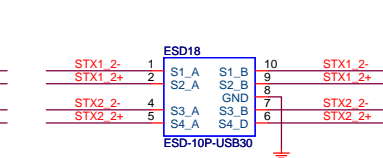
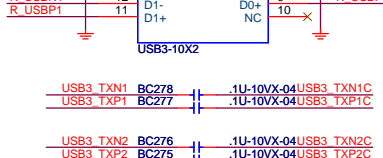
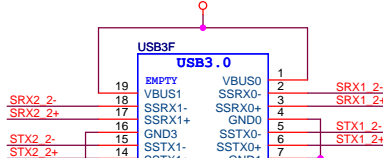
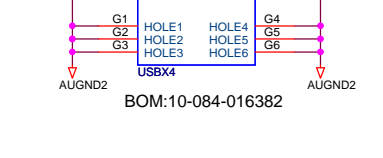
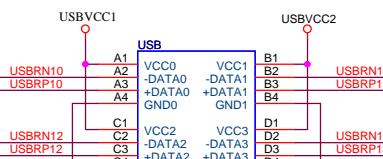
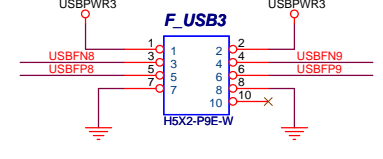
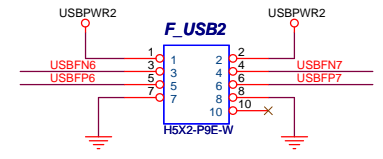
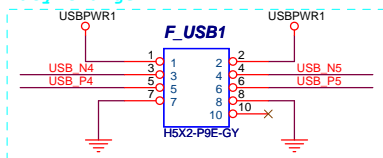


## REAR USB 4 Port

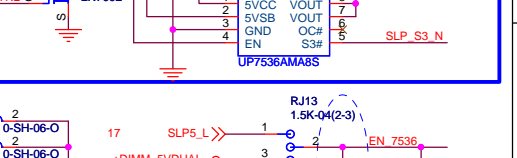
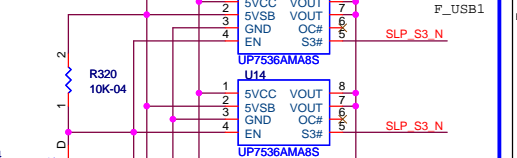
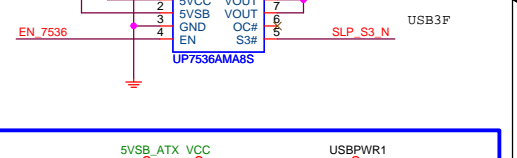
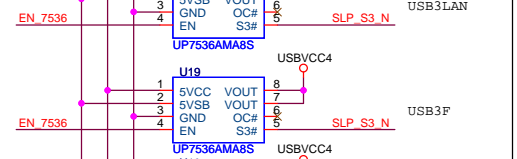
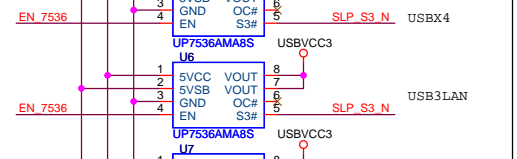
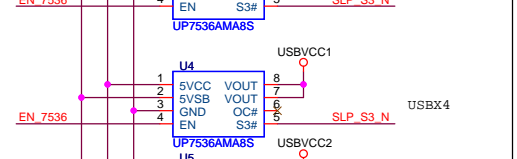
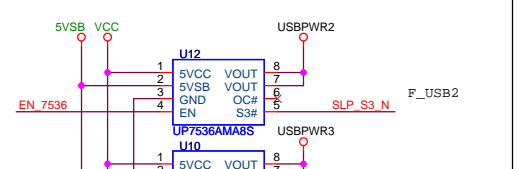
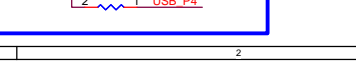
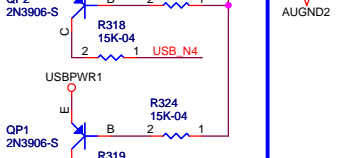
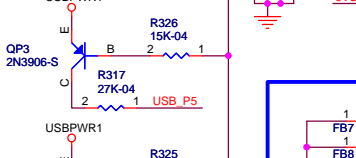
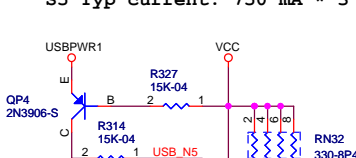
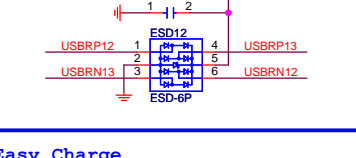
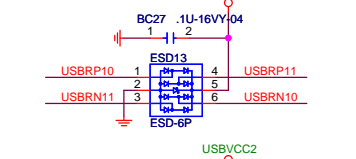
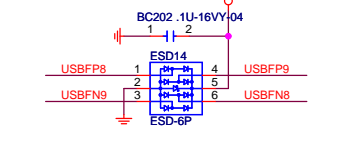
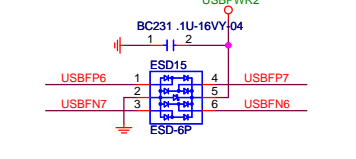
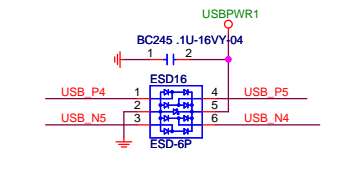


## USB3F

## Easy Charge

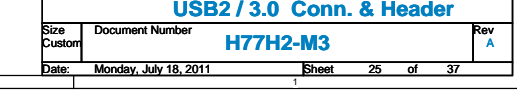
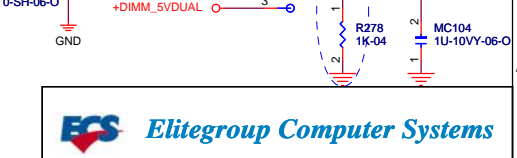
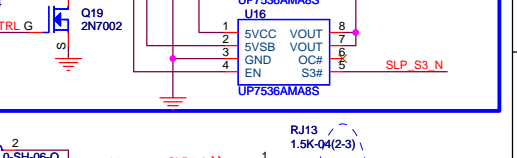
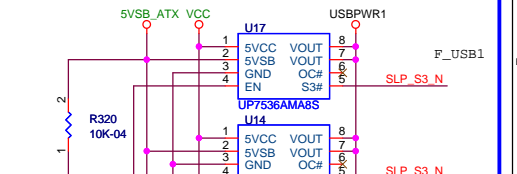
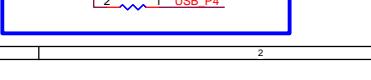
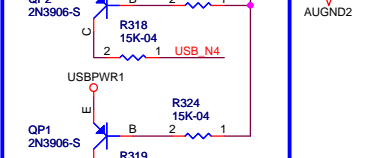
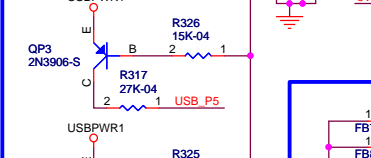
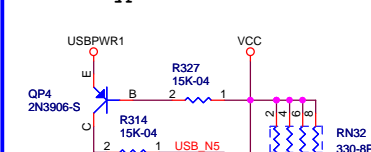


## Close to Header or Connector



## Easy Charge

S5 Typ current: 750 mA \* 3



Elitegroup Computer Systems

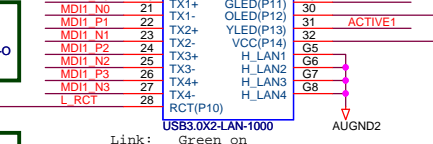
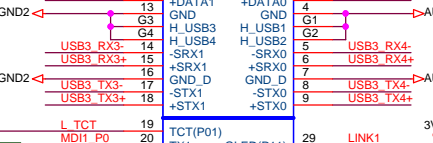
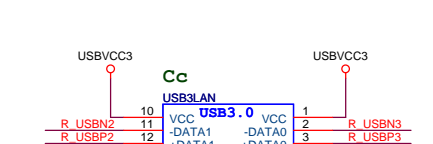
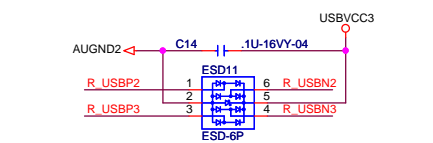
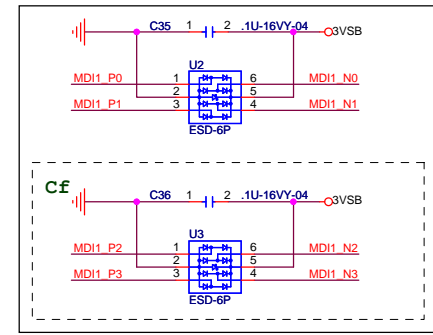
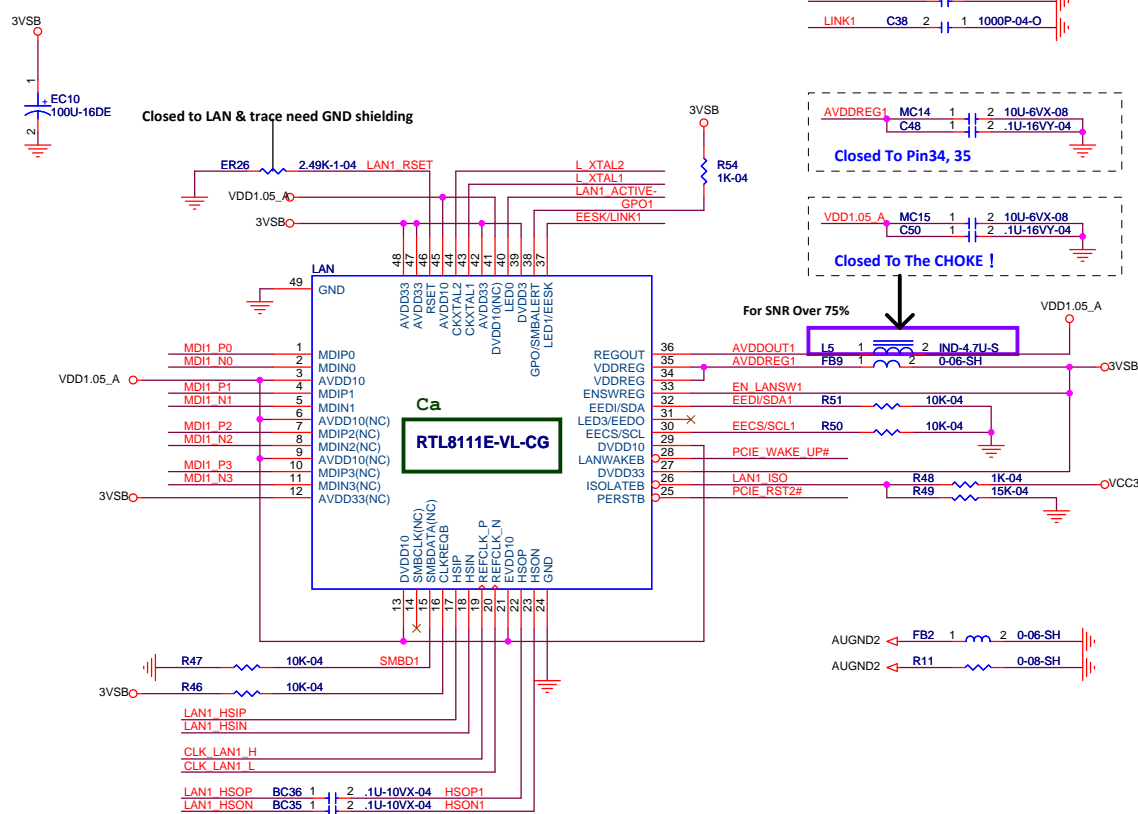
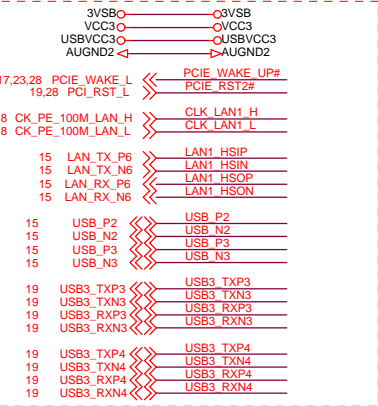
USB2 / 3.0 Conn. & Header

Document Number H77H2-M3

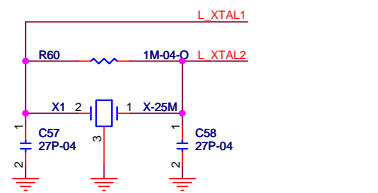
Date: Monday, July 18, 2011 Sheet 25 of 37



External Connection

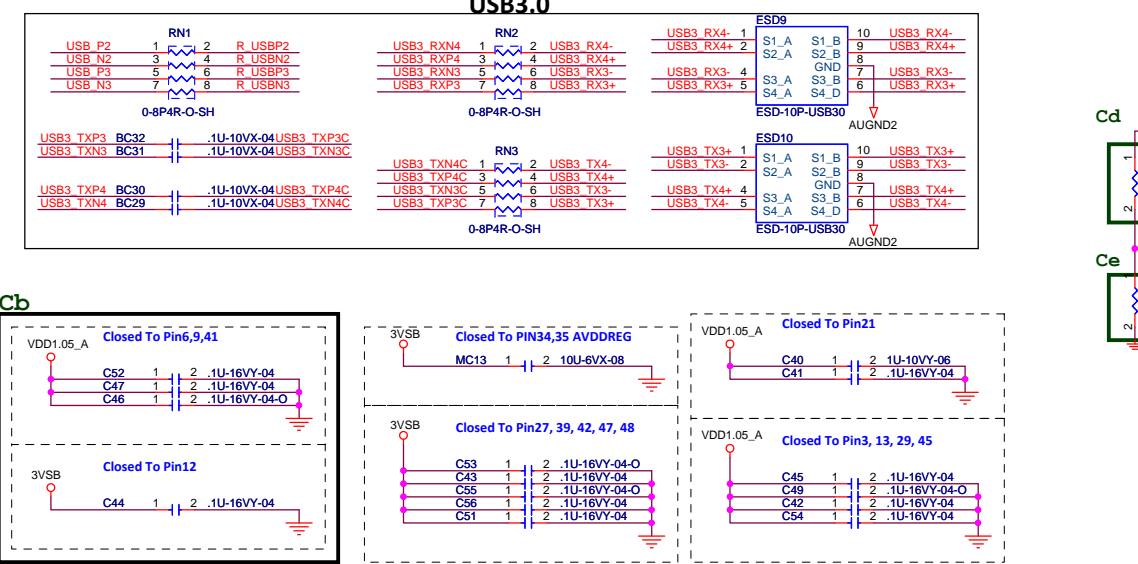


When you found some bug, please inform Ren(ext:26150) to update circuit.  
新手提醒:  
LAN\_HSOP/N請接到SB的PCIE RX端  
LAN\_HSIP/N請接到SB的PCIE TX端  
LAN\_HSIP/N在SB的PCIE TX端要記得放AC coupling cap



BOM Difference	
	RTL8111E-VL 1000M
Ca	RTL8111E-VL-CG
Cb	RTL8105E-VL 10/100M
Cc	USBX2-LAN-1000
Cd	USBX2-LAN-100
Ce	0-04
Cf	0.01U-25VX-04
Cg	

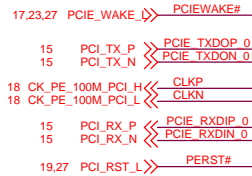
DEFAULT



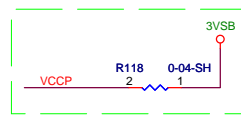
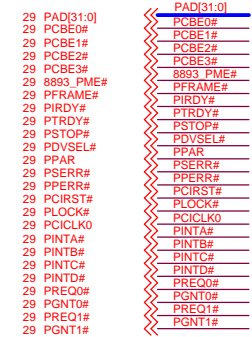
## External Connection



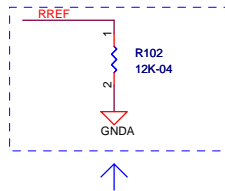
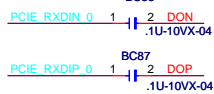
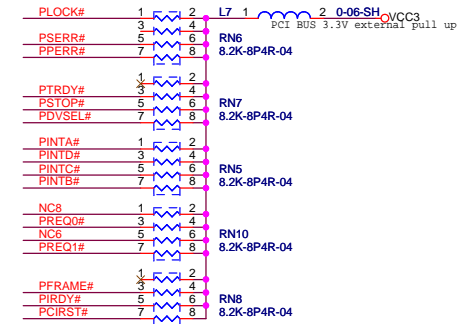
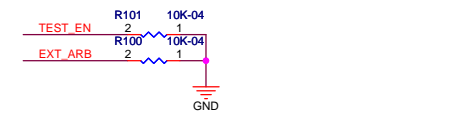
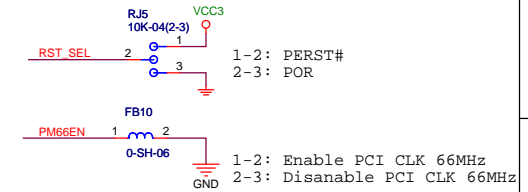
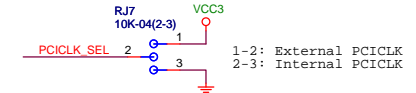
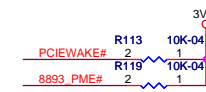
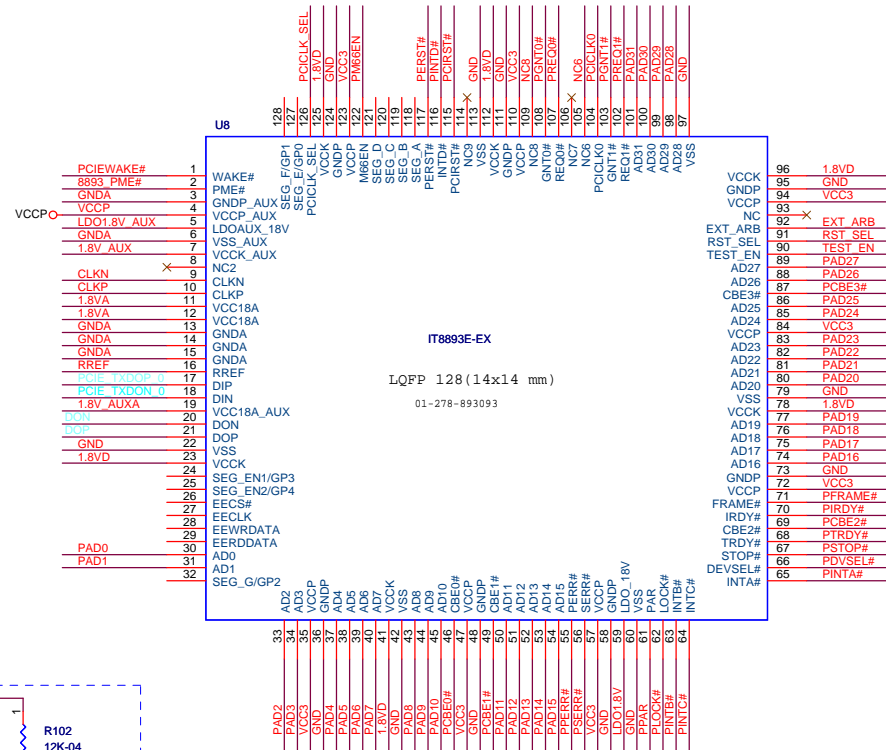
## PCIE



## PCI slot



PCB layout note:  
Connect to PCIE  
PERST# Signal



PCB layout note:  
PCIE TX signals  
Close to chip

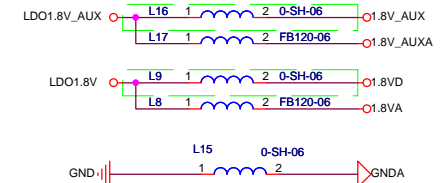
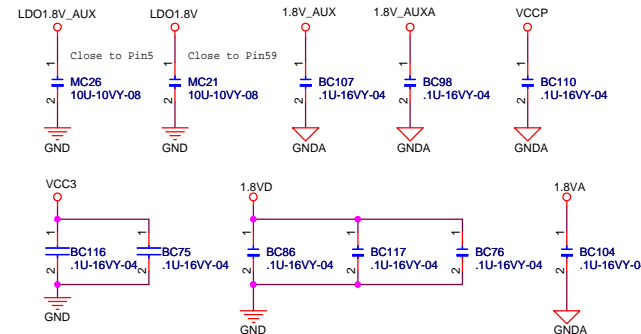
PCB layout note:  
Close to chip

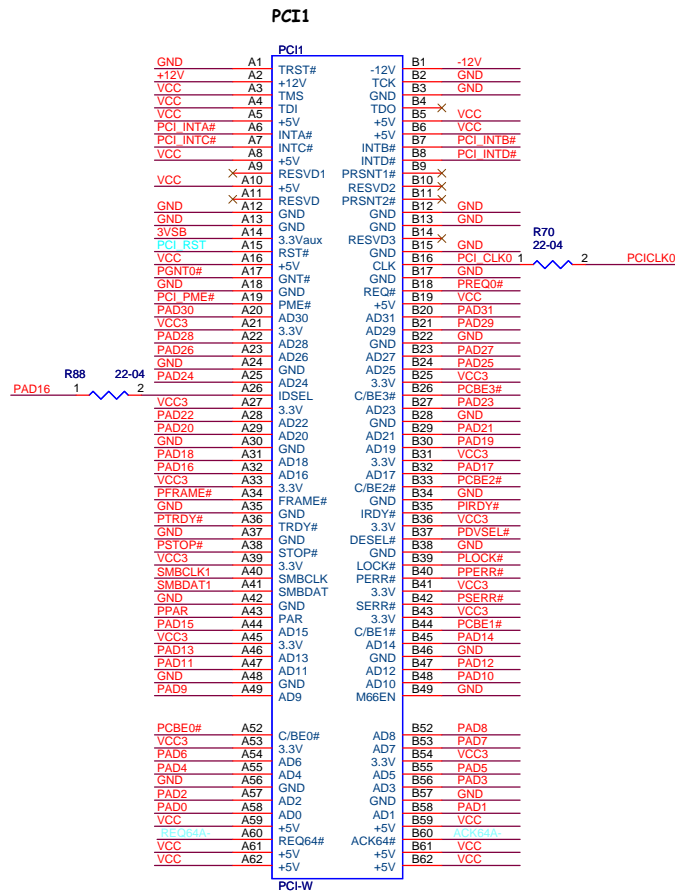
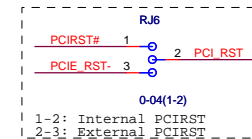
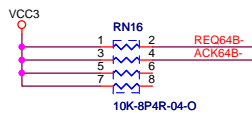
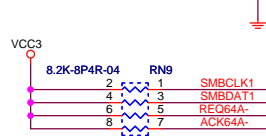
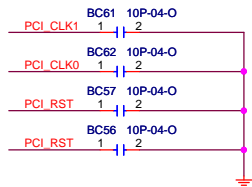
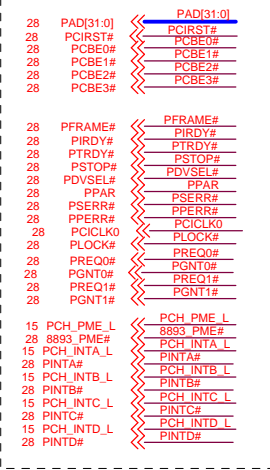
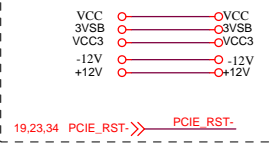
PCIE DIP;DIN;DOP;DON PCB layout note:

To meet Differential Impedance :85 ohm +/- 15%  
To meet Single-ended Impedance :50 ohm +/- 15%  
PCIE DIP and DIN trace width:9.5 mils  
PCIE DOP and DON trace width:9.5 mils  
Space between DIP/DIN and DOP/DON:14.5 mils  
L1 & L2 height:5 mils  
The signal traces Number of vias: 2 (Max.)  
The signal trace above analog GND plane  
Spacing from other groups:>25 mils  
Total trace length: 12 inches (Max.)

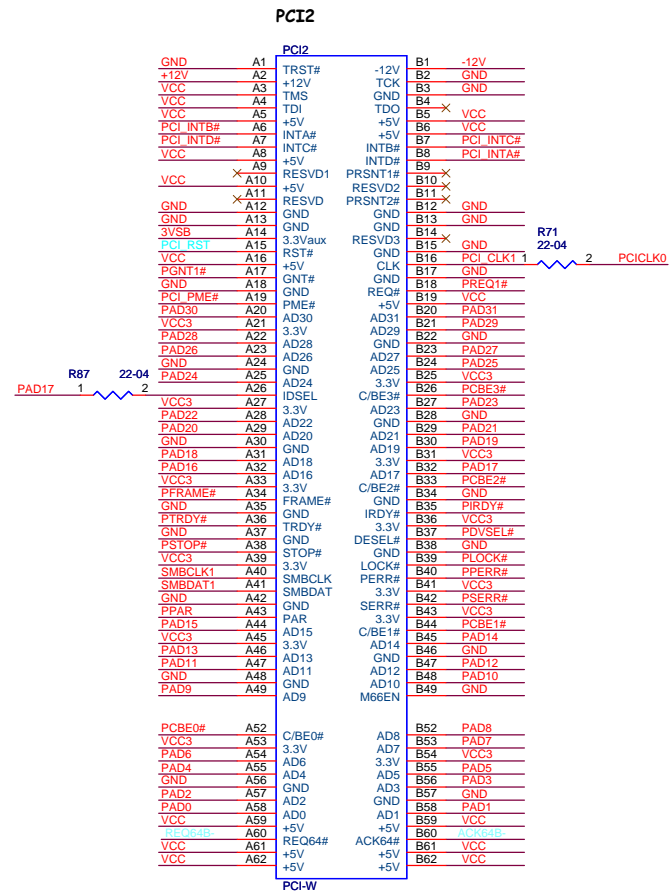
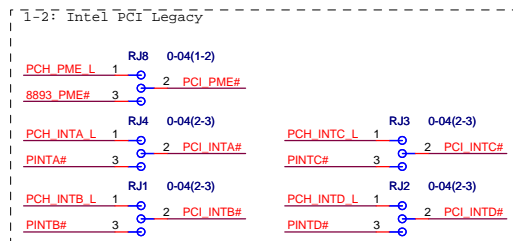
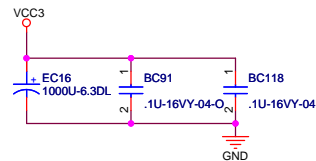
PCIE CLK PCB layout note:

To meet Differential Impedance :100 ohm +/- 15%  
To meet Single-ended Impedance :50 ohm +/- 15%  
CLKP and CLKN trace width:7 mils  
Space between CLKP and CLKN:14 mils  
L1 & L2 height:5 mils  
The signal traces Number of vias: 4 (Max.)  
The signal trace above analog GND plane  
Spacing from other groups:>25 mils  
Total trace length: 12 inches (Max.)

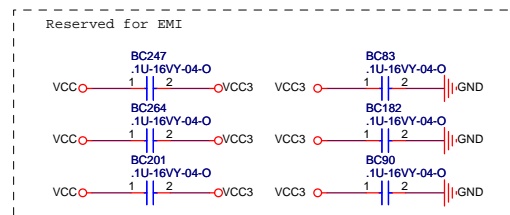
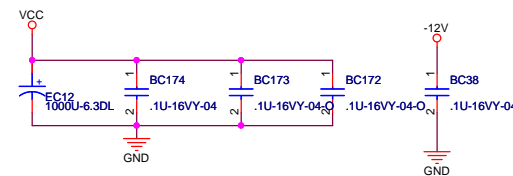




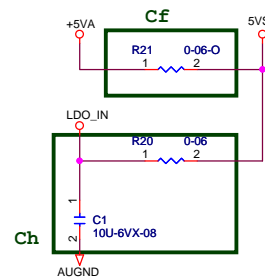
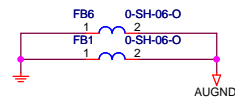
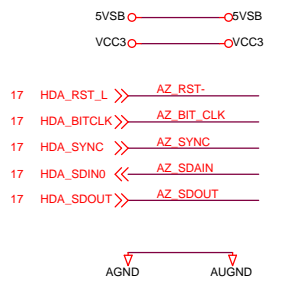
PCI1:REQ0;GNT0 IDSEL:16 INT:ABCD



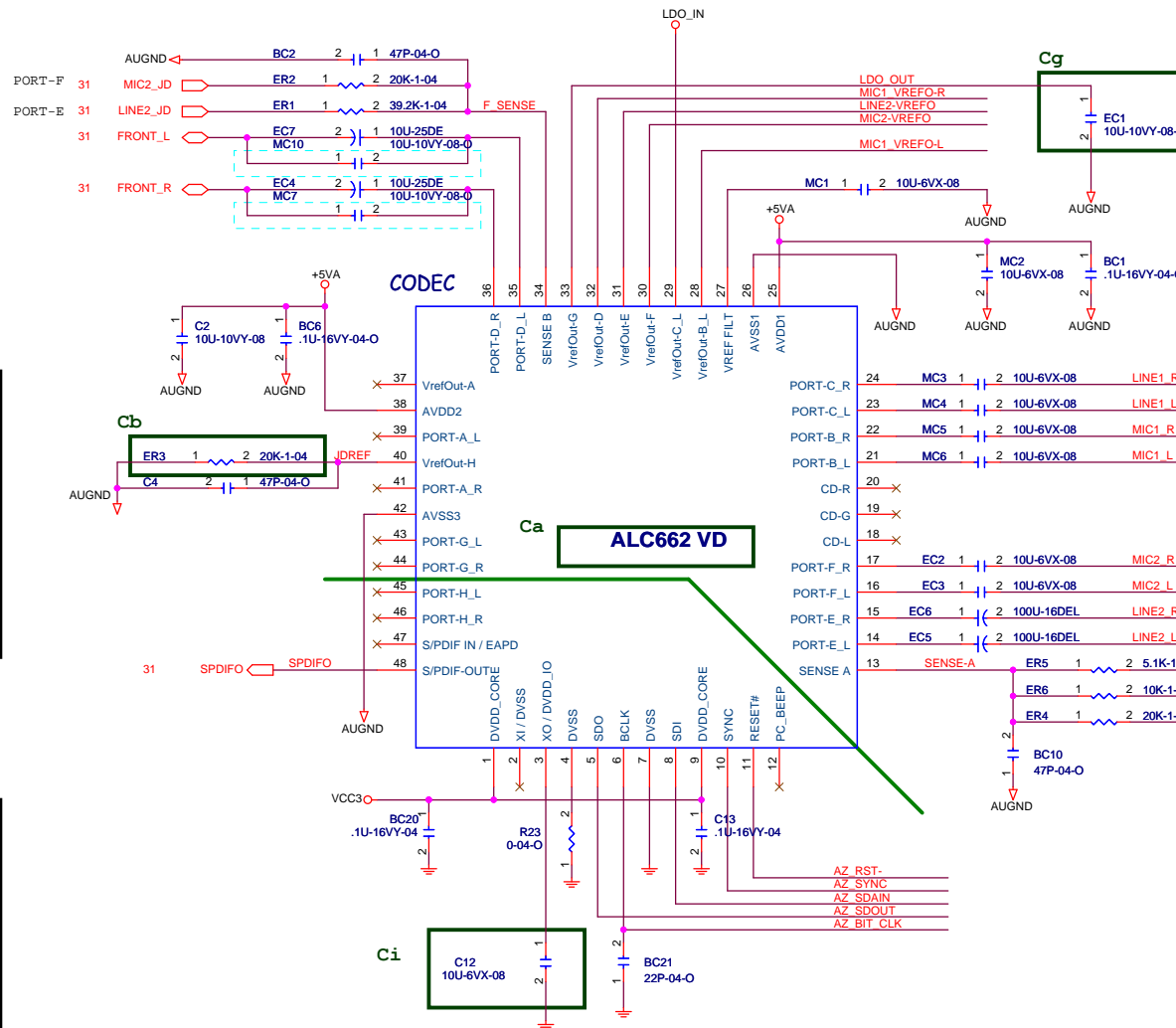
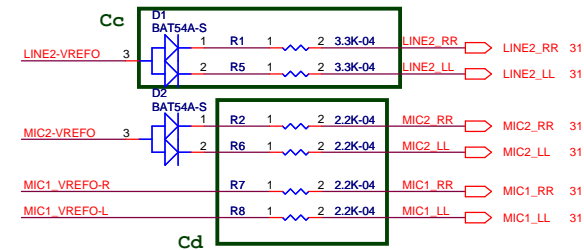
PCI2:REQ1;GNT1 IDSEL:17 INT:BCDA



## External Connection



## MIC Bias



## Pin Difference

Pin	ALC662 VD	VT1705CE
3	REG VREF	GPIOL
4	GPIOL	DVSS
25	LDO OUTPUT	LDO VIN
29	LDO VIN	OPTION CAP
33	LINE1 VREF	LDO OUTPUT
37	FRONT VREF ?	NC
38	LDO OUTPUT	LDO VIN
45	DMIC DATA	NC
46	DMIC CLK	NC

## BOM Difference

Location	ALC662 VD	VT1705CE
Ca	ALC662-VD0-GR	VT1705CE
Cb	20K-1-04	5.1K-1-04
Cc	V	X
Cd	2.2K-04	3.3K-04
Ce	75-04	16-04
Cf	X	V
Cg	X	V
Ch	V	X
Ci	V	X

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

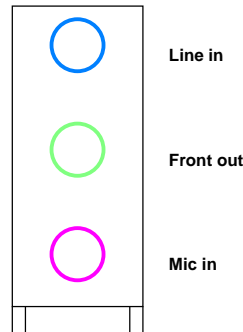
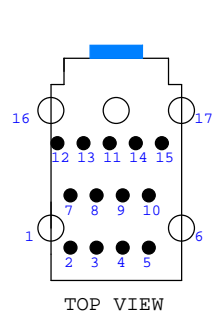
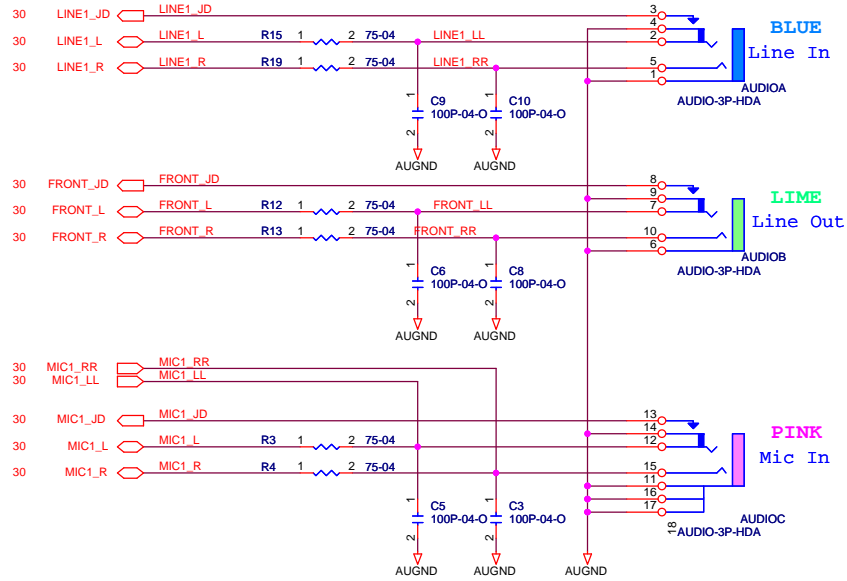


## External Connection

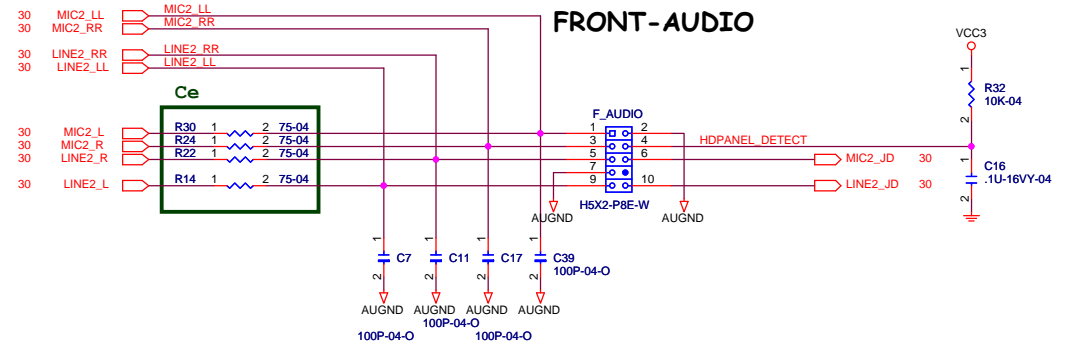
17 FP\_AUD\_DETECT << HDPANEL\_DETECT

\* HDPANEL\_DETECT connect to SIO or SB GPIO for AC97 Panel support

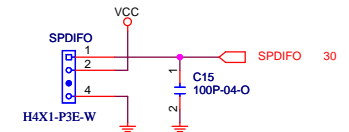
## REAR-AUDIO Non re-tasking for rear panel



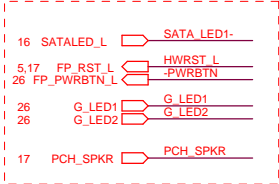
## FRONT-AUDIO



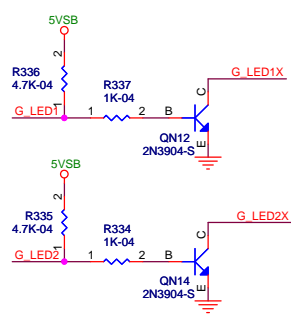
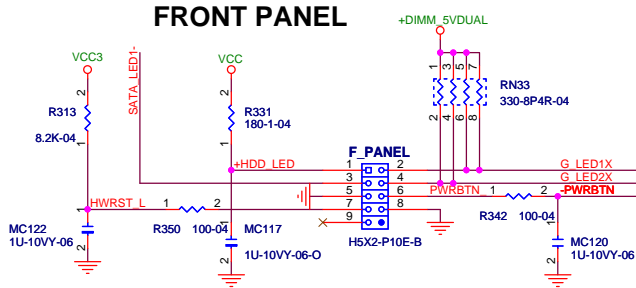
## SPDIF-OUT



External Connection

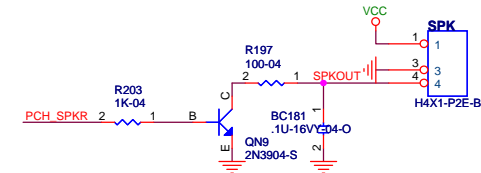


FRONT PANEL



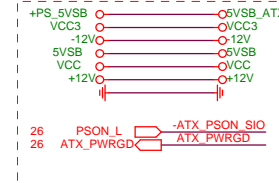
	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
	G	GB	YB	OFF	OFF

B: Blinking

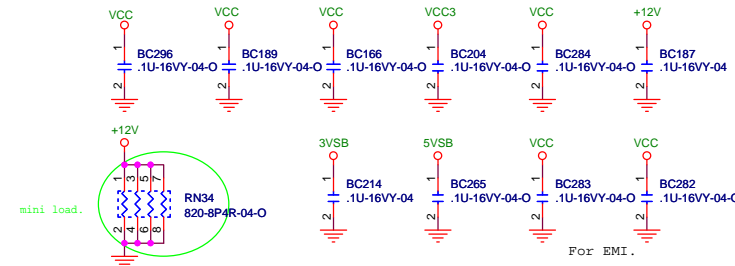
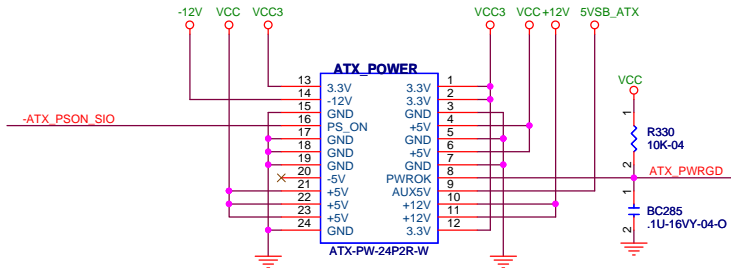


POWER CONNECTOR

External Connection



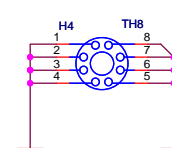
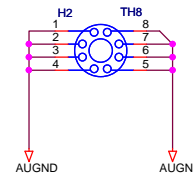
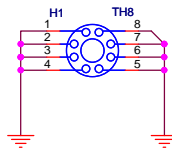
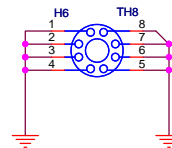
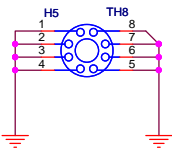
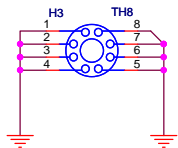
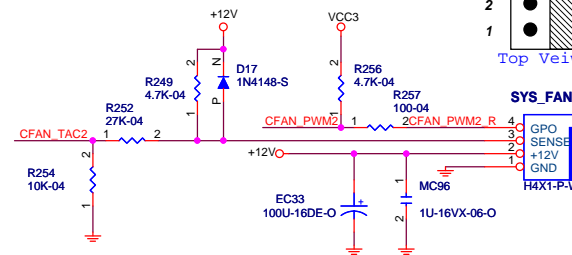
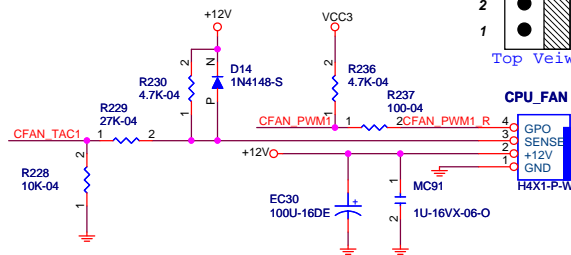
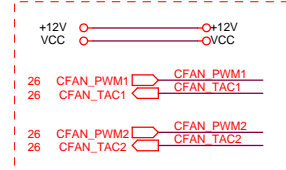
F_PANEL		
1	2	PWR
3	4	
5	6	RST
7	8	
9		



FAN

Kent 1016

External Connection



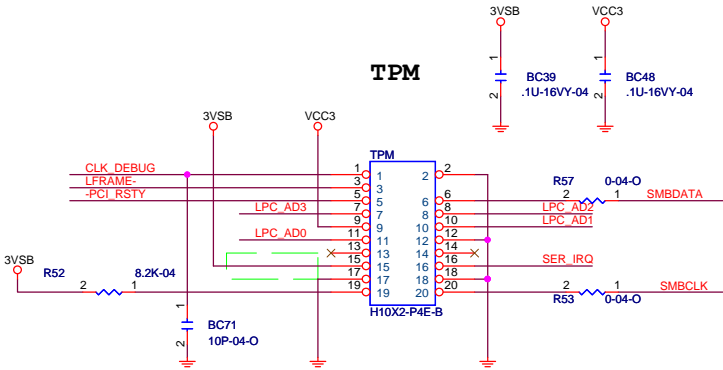
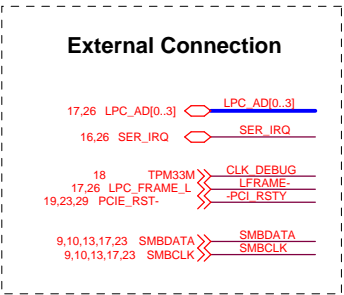
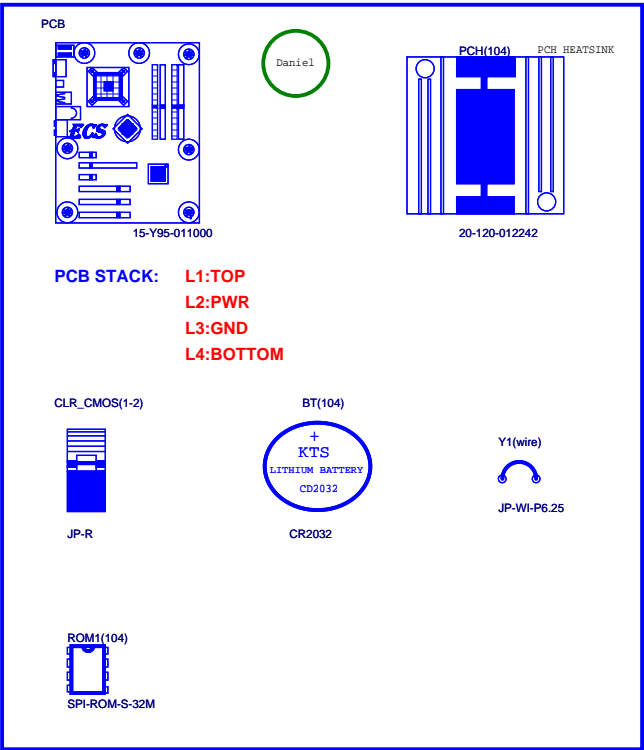
Elitegroup Computer Systems

Title		
F_PANEL / FAN / PWR CONN		
Size	Document Number	Rev
Custom	H77H2-M3	A
Date:	Monday, July 18, 2011	Sheet 32 of 37





104 Phase



1)Circuit type 1

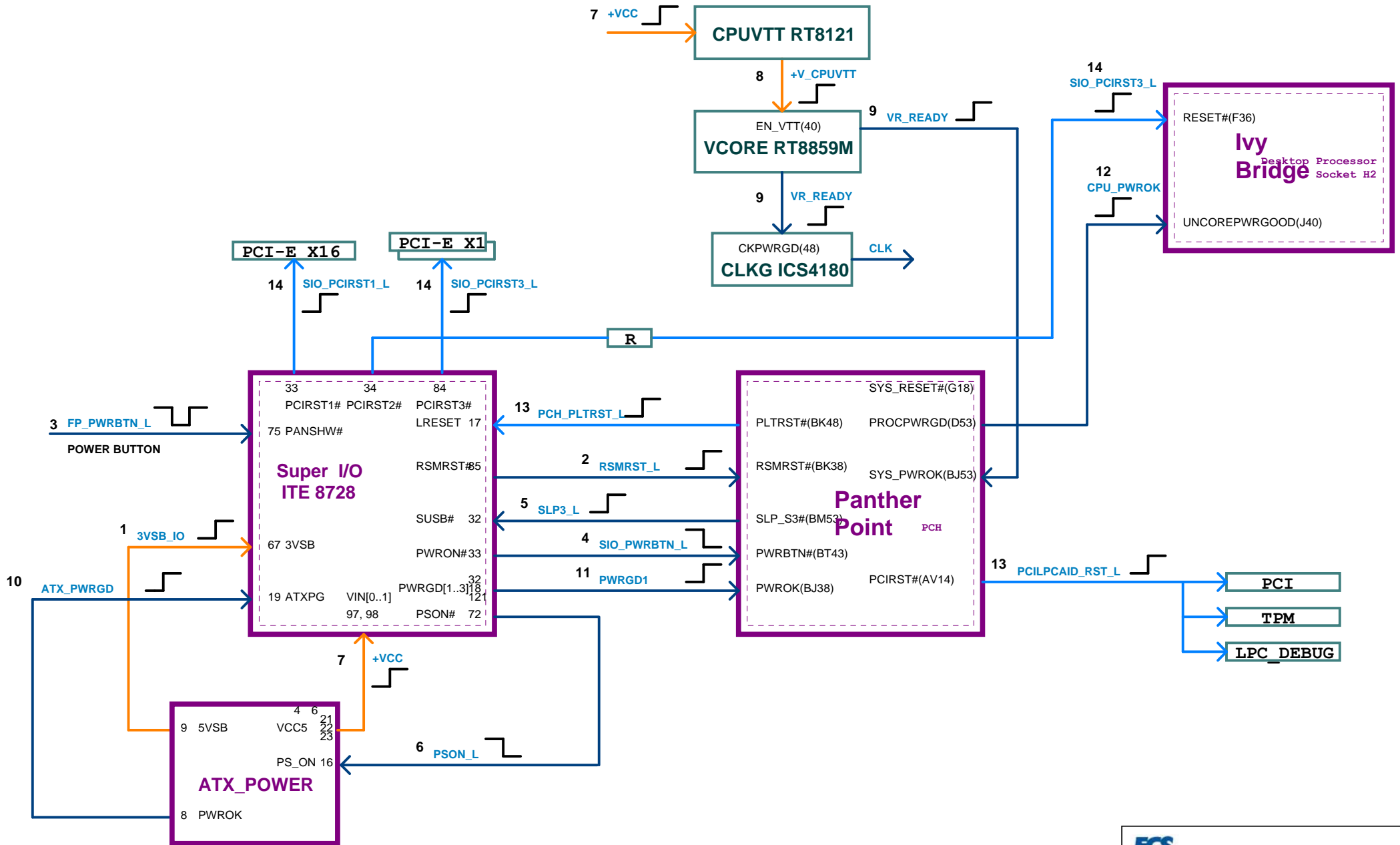
Layer 1:TOP

Layer 2:PWR

Layer 3:GND

Layer 4:BOTTOM





**NOTE:**

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

